Pole-to-ground Fault Analysis for HVDC Grid Based on Common- and Differential-mode Transformation

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***Abstract*—Pole-to-ground (PTG) fault analysis is of vital importance for high-voltage direct current (HVDC) grid. However, many factors are not considered in the existing studies such as the asymmetrical property of PTG fault, the coupling issue between DC transmission lines and the complexity of the structure of DC grid. This paper presents a PTG fault analysis method, which is based on common- and differential-mode (CDM) transformation. Similar to the symmetrical component method in AC system, the transformation decomposes the HVDC grid into CDM networks, which is balanced and decoupled. Then, a transfer impedance is defined and calculated based on the impedance matrices of the CDM networks. With the transfer impedance, analytical expressions of fault characteristics that vary with space and time are obtained. The proposed PTG fault analysis method is applicable to arbitrary HVDC grid topologies, and provides a new perspective to understand the fault mechanism. Moreover, the analytical expressions offer theoretical guidance for PTG fault protection. The validity of the proposed PTG fault analysis method is verified in comparison with the simulation results in PSCAD/EMTDC.**

***Index Terms*—High-voltage direct current (HVDC) grid, pole-to-ground (PTG) fault, common- and differential-mode(CDM) transformation, DC ciruit breaker (DCCB).**

I. Introduction

NOWADAYS, the modular multi-level converter based high-voltage direct current (MMC-HVDC) grid is attractive for renewable power integration [1] and global energy interconnection [2]-[4]. It can be configured by either symmetrical monopole or bipolar structure. Compared with the monopole structure, the symmetrical bipolar configuration shows advantages in bulk power transmission and DC fault-tolerate control [5]. Thus, the symmetrical bipolar based MMC-HVDC grid, which has been recently adopted in the Zhangbei Project, China, becomes the research focus of this paper.

In HVDC grid, the pole-to-ground (PTG) fault is one of the most common DC-side faults. To protect the grid, lots of studies have been conducted, which can be summarized into two solutions [6]-[10]. The first solution is based on MMCs with the handling capability of DC fault. However, this solution needs to block the insulated gate bipolar transistors (IGBTs) [6] or regulate the DC grid voltage to zero [7], [8], which will cause a temporary interruption of the active power transmission. The other solution relies on DC circuit breakers (DCCBs). The faulty DC lines can be selectively isolated with DCCBs, and the healthy DC parts can maintain continuous operation [9], [10]. On this basis, this solution is considered as a promising candidate for future large-scale HVDC grid [2]. Figure 1 shows the typical protection sequence of the DCCB-based solution under PTG fault, where $t_1 \approx 5$ ms; $t_2 \approx 150$ - 500 ms; $t_3 \approx 100$ ms. The transient process is divided into three stages. Stage 1 is fault detecting and DCCB opening; Stage 2 is DC line deionizing; and Stage 3 is DC power flow recovering. Although Stage 1 is quite short (typically around 5 ms), fault transient voltage and current stresses are mainly concentrated in this stage. Thus, PTG fault analysis at Stage 1 can provide theoretical guidance for the selection of DC equipment and the parameter setting of protection relays, which is of vital importance for the HVDC grid.

Aiming at the fault analysis at Stage 1, the numerical and analytical calculations are two effective ways. From the aspect of numerical calculation, some electromagnetic transient (EMT) simulation work is documented in [11], [12], where accurate characteristics of PTG fault are presented. However, this analysis lacks profound understanding of the fault mechanism, and is quite time-consuming, especially for large-scale HVDC grid. As for the analytical calculation, it can theoretically reveal the regularities underlying the fault characteristics. However, there also exist the following difficulties. Firstly, the PTG fault is a typical DC-side asymmetrical fault. The transient voltage and fault current in positive and negative poles are unbalanced. Secondly, with the mutual inductance between DC transmission lines, the fault transient processes of positive and negative poles are coupled. Thirdly, HVDC grid can be constructed with a variety of topolo-

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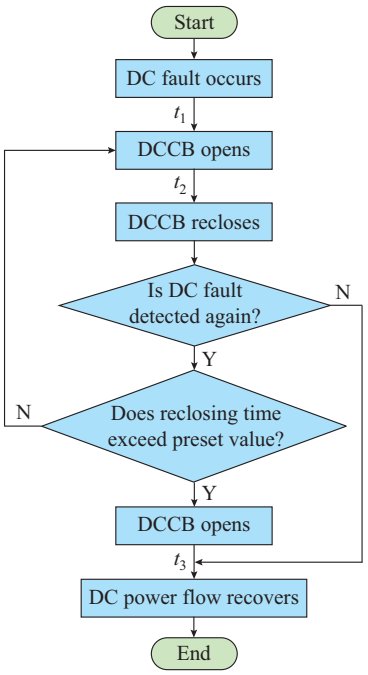
gies including the radial type, the meshed type and a hybrid of the two types. Hence, it is hard to form a unified description that is suitable for arbitrary HVDC grid topologies.



t_1: fault detecting & DCCB opening; t_2: DC line deionizing
t_3: DC power flow recovering

Fig. 1. Typical protection sequence of DCCB-based solution under PTG fault.

The conducted studies focus on the above difficulties in analytical calculation at Stage 1. In line-commutated converter (LCC) based HVDC system, a common- and differential-mode (CDM) transformation is firstly proposed in [13] to overcome the imbalance and coupling issues. Based on that, fault transient overvoltage is analyzed in [13]. Characteristics of the initial values of traveling waves are investigated in [14]. And frequency responses of terminal current and voltage of the converter are presented in [15]. However, these studies merely focus on the two-terminal system, while the complexity of the structure of the DC grid is not considered. Reference [16] proposes a pole-to-pole (PTP) fault current calculation method for MMC-HVDC grid. However, this method is unsuitable for the PTG fault scenario because the attentions are not paid to the factor of mutual inductance.

In this paper, as a further attempt to analytically present the PTG fault characteristics at Stage 1 of the protection sequence, two contributions are made: ① considering the concept of CDM transformation and the complexity of DC grid structure, a generic PTG fault analysis method is proposed, which is suitable for arbitrary HVDC grid topologies; ② based on the proposed method, analytical expressions of the fault characteristics that vary with space and time are derived, which is expected to be applied to the selection of DC protection equipment and parameter setting of protection relays.

The rest of this paper is organized as follows. The basic principle of CDM transformation is introduced in Section II. Based on that, a PTG fault analysis method is proposed in Section III and Section IV gives the analytical expressions of PTG fault characteristics. Then, a simulation study based on Zhangbei Project in China is conducted in Section V for verification. Section VI briefly discusses the practical application of the proposed method of PTG fault analysis. Finally, Section VII draws the conclusions.

II. Basic Principle of CDM Transformation

In LCC-HVDC, the DC-side PTG fault will also cause the imbalance and coupling issues [13]-[15]. The CDM transformation proposed in [13] is an effective tool for analyzing the asymmetrical phenomenon, which shows a similar function as the symmetrical component method in AC system. In this section, the basic principle of CDM transformation is briefly reviewed for a better understanding of the proposed analysis method. Taking DC current as an example, the transformation can be expressed as:

$$\begin{bmatrix} i^{\Sigma} \\ i^{\Delta} \end{bmatrix} = \frac{1}{2}\begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix}\begin{bmatrix} i_p \\ i_n \end{bmatrix} \tag{1}$$

where the subscripts p and n are the positive and negative pole components, respectively; and the superscripts Σ and Δ are the CDM components. With the transformation, a pair of unbalanced positive and negative pole currents can be decomposed into two couples of balanced CDM components. This property is employed in the following sections to analyze the PTG fault.

III. CDM Transformation Based PTG Fault Analysis Method

In this section, based on the CDM transformation, a PTG fault analysis method is proposed. The main idea contains two aspects. Firstly, to address the imbalance and coupling issues, the HVDC grid is transferred into CDM networks. Secondly, from the perspective of CDM components, a transfer impedance based analysis is performed. Thus the analytical expression of the PTG fault point current is obtained. Figure 2(a) shows an arbitrary HVDC grid. It contains n nodes and b branches. The nodes consist of m active nodes (with MMC connected) and $n-m$ passive nodes (without MMC connected). Without the loss of generality, a PTG fault is assumed to occur at the negative pole of DC line. The fault point is defined as the $(n+1)^{\text{th}}$ node.

A. CDM Transformation of HVDC Grid

1) DC Transmission Lines

The DC transmission line can be modeled as the distributed frequency-dependent (FD) model [14]-[16] or the lumped RL model [17], [18]. Figure 3 shows a comparison of DC fault current when the lumped RL model and the distributed FD model are adopted. Figure 3(a) is in the scenario of low-fault resistance (0.01 Ω) while Fig. 3(b) is in the scenario of high-fault resistance (15 Ω). It is found that the fault current employing the lumped RL model is the average approximation of the fault current employing distributed FD model. Moreover, although transient oscillation is observed in the scenario adopting FD model, it decays with time. And the at-

tenuation of the oscillation trends to be more obvious in the scenario of large fault resistance. Based on the aforementioned average approximation and the attenuation effect, the transient oscillation has little impact on the calculation of the maximum fault current value. Thus, the lumped RL model, previously used in [17], [18], is adopted in this paper for the current stress estimation.

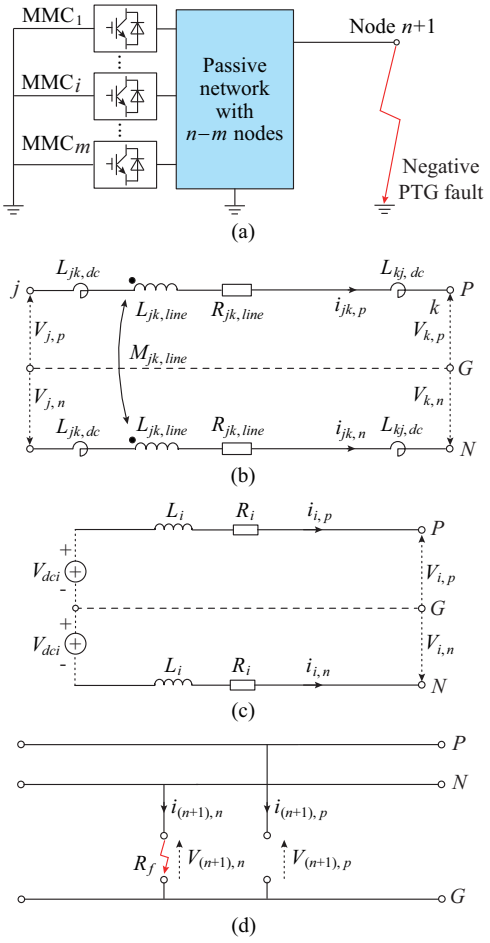


Fig. 2. Symmetrical bipolar based MMC-HVDC grid. (a) Grid Topology. (b) DC transmission line. (c) MMC station. (d) Fault boundary condition.

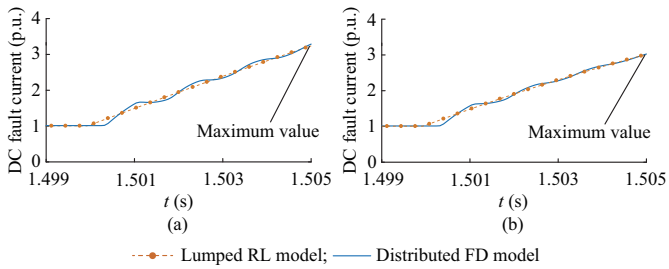


Fig. 3. DC fault current comparison under different fault resistance scenarios. (a) Fault resistance is 0.01 Ω. (b) Fault resistance is 15 Ω.

Figure 2(b) shows the RL model of DC transmission line, where nodes j and k are the terminals of the transmission line; G represents the ground; V_j and V_k are the voltages (with respect to ground) of nodes j and k, respectively; i_{jk} is the branch current; $L_{jk,line}$ and $M_{jk,line}$ are the self and mutual inductances of branch jk, respectively; $R_{jk,line}$ is the line resistance; and $L_{jk,dc}$ and $L_{kj,dc}$ are the DC reactors close to node j and node k, respectively. Based on Fig. 2(b), the KVL equation is written as:

$$\begin{bmatrix} V_{j,p}-V_{k,p} \\ V_{j,n}-V_{k,n} \end{bmatrix} = R_{jk,line}\begin{bmatrix} i_{jk,p} \\ i_{jk,n} \end{bmatrix} + \begin{bmatrix} L_{jk,dc}+L_{kj,dc}+L_{jk,line} & M_{jk,line} \\ M_{jk,line} & L_{jk,dc}+L_{kj,dc}+L_{jk,line} \end{bmatrix} \frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_{jk,p} \\ i_{jk,n} \end{bmatrix} \quad (2)$$

In (2), the non-diagonal elements of the coefficient matrix are not zero, which implies the coupling of positive and negative poles. Thus, the PTG fault characteristics cannot be solved independently from positive or negative poles. To address the problem, the transformation in (1) is applied, and (2) is transferred to (3):

$$\begin{cases} \begin{bmatrix} V_j^{\Sigma}-V_k^{\Sigma} \\ V_j^{\Delta}-V_k^{\Delta} \end{bmatrix} = R_{jk,line}\begin{bmatrix} i_{jk}^{\Sigma} \\ i_{jk}^{\Delta} \end{bmatrix} + \begin{bmatrix} L_{jk,dc}+L_{kj,dc}+L_{jk,line}^{\Sigma} & 0 \\ 0 & L_{jk,dc}+L_{kj,dc}+L_{jk,line}^{\Delta} \end{bmatrix} \frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_{jk}^{\Sigma} \\ i_{jk}^{\Delta} \end{bmatrix} \\ L_{jk,ine}^{\Sigma} = L_{jk,line}+M_{jk,line} \\ L_{jk,line}^{\Delta} = L_{jk,line}-M_{jk,line} \end{cases} \quad (3)$$

It can be observed that (3) is under the perspective of CDM components, where the coupling terms in the coefficient matrix have disappeared.

2) MMC Stations

As indicated in Section I, this study focuses on Stage 1 of the PTG fault protection sequence (about 5 ms). At this stage, the MMC station is still in the normal operation mode. Some fault transient controls such as the blocking and fault ride through control, do not need to be considered. In [19], the RLC model is employed to calculate the fault characteristics of MMC. However, further elaboration presents that the voltage variation of DC-side equivalent capacitor at this stage is within 0.1 p.u., as listed in the Appendix A. Hence, the RLC model can be further equivalent to an RL model, as shown in Fig. 2(c), where V_{dci} is the rated DC voltage; i_i is the DC current; and R_i and L_i are the DC-side equivalent resistance and inductance, respectively. The subscript i represents the i^{th} $(i=1,2,\ldots,m)$ MMC station. Figure 4 shows the DC fault current comparison between RL model and detailed switching model in different operation modes. The comparison is under the precondition that the MMC is not blocked (arm currents are limited to 1.7 p.u.). It is found that during the initial 5 ms, the maximum error between the two modes is within 10%. Thus, it is accurate enough to estimate the fault current of MMC by RL model.

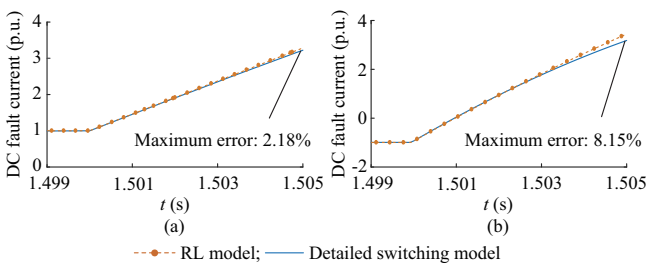


Fig. 4. DC fault current comparison between RL model and detailed switching model. (a) Rectifier operation mode. (b) Inverter operation mode.

Based on Fig. 2(c), the KVL equation can be written as:

$$\begin{bmatrix} V_{i,p} \\ V_{i,n} \end{bmatrix} = \begin{bmatrix} V_{dci} \\ -V_{dci} \end{bmatrix} - L_i \frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} i_{i,p} \\ i_{i,n} \end{bmatrix} - R_i \begin{bmatrix} i_{i,p} \\ i_{i,n} \end{bmatrix} \tag{4}$$

With CDM transformation, (4) is transferred as:

$$\begin{bmatrix} V_i^{\Sigma} \\ V_i^{\Delta} \end{bmatrix} = \begin{bmatrix} 0 \\ V_{dci}^{\Delta} \end{bmatrix} - L_i \frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} i_i^{\Sigma} \\ i_i^{\Delta} \end{bmatrix} - R_i \begin{bmatrix} i_i^{\Sigma} \\ i_i^{\Delta} \end{bmatrix} \tag{5}$$

3) Fault Boundary Condition

When a negative PTG fault occurs, the fault boundary condition is depicted in Fig. 2(d). It can be expressed as:

$$\begin{cases} i_{(n+1),p} = 0 \\ V_{(n+1),n} = R_f i_{(n+1),n} \end{cases} \tag{6}$$

where R_f is the fault resistance. Transforming (6) into its CDM components, we can obtain:

$$\begin{cases} i_{(n+1)}^{\Sigma} + i_{(n+1)}^{\Delta} = 0 \\ V_{(n+1)}^{\Sigma} - V_{(n+1)}^{\Delta} = R_f \left(i_{(n+1)}^{\Sigma} - i_{(n+1)}^{\Delta} \right) \end{cases} \tag{7}$$

Then, combining (3), (5) and (7), the transformed DC transmission lines, MMC stations and PTG fault boundary condition constitute the CDM networks, as shown in Fig. 5. At this point, from the perspective of CDM components, the imbalance and coupling issues do not exist, which is of benefit to the following analysis of PTG fault.

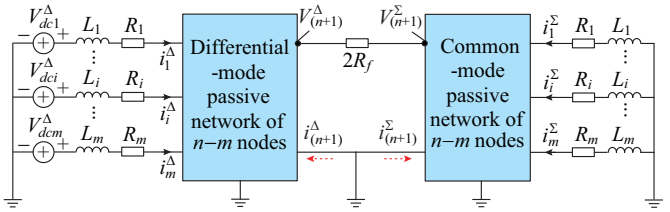


Fig. 5. CDM networks.

B. Impedance Matrix Deduction of CDM Networks

In this part, the impedance matrices of CDM networks are derived. Firstly, the admittance of DC lines and MMC stations are expressed in the form of $1/(Ls+R)$, where s is the Laplace operator. Then, based on the structure of HVDC grid, the admittance matrices of CDM networks are written as $\boldsymbol{Y}^{\Sigma}$ and $\boldsymbol{Y}^{\Delta}$. By inverting $\boldsymbol{Y}^{\Sigma}$ and $\boldsymbol{Y}^{\Delta}$, the impedance matrices can be obtained.

$$\boldsymbol{Z}^{\Sigma} = (\boldsymbol{Y}^{\Sigma})^{-1} = \begin{bmatrix} Z_{11}^{\Sigma} & Z_{12}^{\Sigma} & \cdots & Z_{1(n+1)}^{\Sigma} \\ Z_{21}^{\Sigma} & Z_{22}^{\Sigma} & \cdots & Z_{2(n+1)}^{\Sigma} \\ \vdots & \vdots & & \vdots \\ Z_{(n+1)1}^{\Sigma} & Z_{(n+1)2}^{\Sigma} & \cdots & Z_{(n+1)(n+1)}^{\Sigma} \end{bmatrix} \tag{8}$$

$$\boldsymbol{Z}^{\Delta} = (\boldsymbol{Y}^{\Delta})^{-1} = \begin{bmatrix} Z_{11}^{\Delta} & Z_{12}^{\Delta} & \cdots & Z_{1(n+1)}^{\Delta} \\ Z_{21}^{\Delta} & Z_{22}^{\Delta} & \cdots & Z_{2(n+1)}^{\Delta} \\ \vdots & \vdots & & \vdots \\ Z_{(n+1)1}^{\Delta} & Z_{(n+1)2}^{\Delta} & \cdots & Z_{(n+1)(n+1)}^{\Delta} \end{bmatrix} \tag{9}$$

However, it should be noted that the Laplace operator s in $\boldsymbol{Y}^{\Sigma}$ and $\boldsymbol{Y}^{\Delta}$ cannot be substituted by $j\omega$ directly since Stage 1 of the PTG fault protection sequence is a transient process. As a result, the inverting process will be very complicated if the grid resistance is considered.

Fortunately, the voltage drop on the grid resistors, including the DC-side equivalent resistor of the converter and the DC line resistor, is much smaller than those on the inductors during Stage 1. Thus, the grid resistors are neglected in this paper, and the inverting process of admittance matrices is largely simplified.

C. Transfer Impedance Based PTG Fault Analysis

According to the superposition theorem, the voltage of $(n+1)^{\text{th}}$ node can be expressed as the sum of the voltage generated by each fault excitation source. Thus, based on Fig. 5, the voltage of the fault point is written as:

$$V_{(n+1)}^{\Delta} = \sum_{i=1}^{m} \frac{V_{dci}^{\Delta}}{z_i^{\Delta}} Z_{i(n+1)}^{\Delta} - Z_{(n+1)(n+1)}^{\Delta} i_{(n+1)}^{\Delta} \tag{10}$$

where z_i is the DC-side equivalent impedance of the i^{th} MMC station. Meanwhile, the relation between $V_{(n+1)}^{\Delta}$ and $i_{(n+1)}^{\Delta}$ can also be expressed as:

$$i_{(n+1)}^{\Delta} = -i_{(n+1)}^{\Sigma} = \frac{V_{(n+1)}^{\Delta}}{2R_f + Z_{(n+1)(n+1)}^{\Sigma}} \tag{11}$$

Substituting (10) into (11), we can obtain:

$$i_{(n+1)}^{\Delta} = -i_{(n+1)}^{\Sigma} = \frac{\sum_{i=1}^{m} V_{dci}^{\Delta} Z_{i(n+1)}^{\Delta} / z_i^{\Delta}}{2R_f + Z_{(n+1)(n+1)}^{\Sigma} + Z_{(n+1)(n+1)}^{\Delta}} \tag{12}$$

Then, the transfer impedance $z_{js,i}$ is defined as:

$$z_{js,i} = z_i^{\Delta} \left(2R_f + Z_{(n+1)(n+1)}^{\Sigma} + Z_{(n+1)(n+1)}^{\Delta} \right) / Z_{i(n+1)}^{\Delta} \tag{13}$$

Hence, (12) is simplified as:

$$i_{(n+1)}^{\Delta} = -i_{(n+1)}^{\Sigma} = \sum_{i=1}^{m} V_{dci}^{\Delta} / z_{js,i} \tag{14}$$

The value of $z_{js,i}$ is determined by the structure and parameters of the HVDC grid, which can be calculated by the deduced impedance matrices. From (14), it is seen that the analytical expression of fault current can be acquired as long as the transfer impedance is calculated. But (14) is expressed in frequency domain. To obtain the analytical expression in time domain, the calculated transfer impedance $z_{js,i}$ is rewritten in form of $(R_{js,i}+sL_{js,i})$, where $R_{js,i}$ and $L_{js,i}$ are the equivalent resistance and inductance of $z_{js,i}$, respectively. Thus, the PTG fault current in time domain is deduced as:

$$i_{(n+1)}^{\Delta} = -i_{(n+1)}^{\Sigma} = \sum_{i=1}^{m} \frac{V_{dci}}{R_{js,i}} \left(1 - \mathrm{e}^{-\left(R_{js,i} / L_{js,i} \right) t} \right) \tag{15}$$

IV. Analytical Expressions of PTG Fault Transient Voltage and Current

Section III proposes a CDM transformation based PTG fault analysis method, where the analytical expression of fault point current that varies with time is obtained. In this section, further analysis of the fault characteristics that vary with space is presented.

A. Distribution of Fault Transient Voltage in HVDC Grid

In this part, the distribution of fault transient voltage along arbitrary branch is deduced. As shown in Fig. 6, x is

defined as the ratio between the distance from the studied point to the branch node with the largest index and the total branch length. The transient voltage of any node in the CDM networks can be derived as the sum of its initial value and the voltage increment which is generated by the fault current:

$$V_i^{\Sigma} = V_{i,0}^{\Sigma} - i_{(n+1)}^{\Sigma} Z_{i(n+1)}^{\Sigma} \tag{16}$$

$$V_i^{\Delta} = V_{i,0}^{\Delta} - i_{(n+1)}^{\Delta} Z_{i(n+1)}^{\Delta} \tag{17}$$

where the subscript 0 means the initial value. It can be obtained with the steady-state power flow calculation method [20]. Thus, the distribution of fault transient voltages along branch *jk* is written as:

$$V_x^{\Delta} = \frac{L_{jk,dc} + (1-x) L_{jk,line}^{\Delta}}{L_{jk}^{\Delta}} V_k^{\Delta} + \frac{L_{kj,dc} + x L_{jk,line}^{\Delta}}{L_{jk}^{\Delta}} V_j^{\Delta} \tag{18}$$

$$V_x^{\Sigma} = \frac{L_{jk,dc} + (1-x) L_{jk,line}^{\Sigma}}{L_{jk}^{\Sigma}} V_k^{\Sigma} + \frac{L_{kj,dc} + x L_{jk,line}^{\Sigma}}{L_{jk}^{\Sigma}} V_j^{\Sigma} \tag{19}$$

where L_{jk} is the inductance of branch *jk* with the consideration of DC reactors, satisfying $L_{jk}^{\Sigma} = L_{jk,dc} + L_{kj,dc} + L_{jk,line}^{\Sigma}$ and $L_{jk}^{\Delta} = L_{jk,dc} + L_{kj,dc} + L_{jk,line}^{\Delta}$.

Then, with inverse CDM transformation, the transient voltages in positive and negative poles are obtained as:

$$\begin{cases} V_{x,p} = V_x^{\Sigma} + V_x^{\Delta} \\ V_{x,n} = V_x^{\Sigma} - V_x^{\Delta} \end{cases} \tag{20}$$

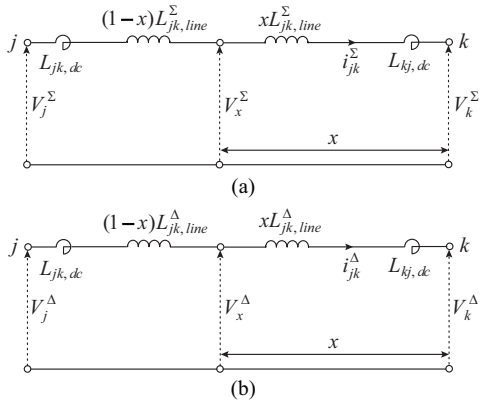


Fig. 6. Distribution of fault transient voltage along branch *jk*. (a) Common-mode branch. (b) Differential-mode branch.

B. Distribution of Fault Current in HVDC Grid

In this part, the arbitrary branch current in the HVDC grid is deduced. Based on (18) and (19), any branch current in CDM networks can be acquired. Take branch *jk* as an example, we can obtain:

$$i_{jk}^{\Sigma} = \frac{V_j^{\Sigma} - V_k^{\Sigma}}{z_{jk}^{\Sigma}} = i_{jk,0}^{\Sigma} - i_{(n+1)}^{\Sigma} \frac{Z_{j(n+1)}^{\Sigma} - Z_{k(n+1)}^{\Sigma}}{z_{jk}^{\Sigma}} \tag{21}$$

$$i_{jk}^{\Delta} = \frac{V_j^{\Delta} - V_k^{\Delta}}{z_{jk}^{\Delta}} = i_{jk,0}^{\Delta} - i_{(n+1)}^{\Delta} \frac{Z_{j(n+1)}^{\Delta} - Z_{k(n+1)}^{\Delta}}{z_{jk}^{\Delta}} \tag{22}$$

where z_{jk} is the impedance of branch *jk*, satisfying $z_{jk}=sL_{jk}$. For branches that connect active node *i* (i=1, 2, ..., m) and the ground, (21) and (22) are also applicable and can be rewritten as:

$$i_i^{\Sigma} = \frac{-V_i^{\Sigma}}{z_i^{\Sigma}} = i_{i,0}^{\Sigma} + i_{(n+1)}^{\Sigma} \frac{Z_{i(n+1)}^{\Sigma}}{z_i^{\Sigma}} \tag{23}$$

$$i_i^{\Delta} = \frac{-V_i^{\Delta}}{z_i^{\Delta}} = i_{i,0}^{\Delta} + i_{(n+1)}^{\Delta} \frac{Z_{i(n+1)}^{\Delta}}{z_i^{\Delta}} \tag{24}$$

Thus, with inverse CDM transformation, the fault currents in positive and negative poles are obtained:

$$\begin{cases} i_{jk,p} = i_{jk}^{\Sigma} + i_{jk}^{\Delta} \\ i_{jk,n} = i_{jk}^{\Sigma} - i_{jk}^{\Delta} \end{cases} \tag{25}$$

$$\begin{cases} i_{i,p} = i_i^{\Sigma} + i_i^{\Delta} \\ i_{i,n} = i_i^{\Sigma} - i_i^{\Delta} \end{cases} \tag{26}$$

Although (25) and (26) do not involve the space variable *x*, they are the fault currents at different DC lines in the CDM networks, which still contain the space information.

V. Comparative Study with Simulation

To verify the validity of the proposed fault analysis method, a symmetrical bipolar four-terminal MMC-HVDC grid is built in PSCAD/EMTDC. It is based on Zhangbei Project in China, and its configuration is shown in Fig. 7. The MMC station employs the average value model, which can reduce the computational efforts with satisfactory accuracy [21]. The configuration of the average value model is depicted in Appendix B, and parameters of the MMC stations are listed in Table I.

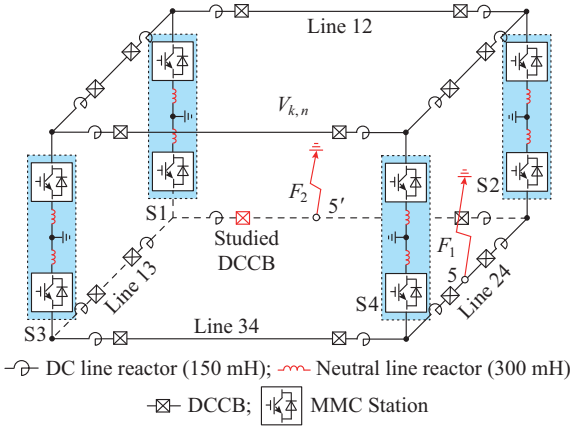


Fig. 7. Symmetrical bipolar based four-terminal MMC-HVDC grid.

TABLE I
Parameters of MMC Stations

Parameter	Value			
	S1	S2	S3	S4
Rated DC voltage (kV)	±500	±500	±500	±500
Rated AC voltage (kV)	260	260	260	260
Rated active power (MW)	1500	−1500	3000	−3000
Rated reactive power (Mvar)	−300	−300	−600	−600
Number of SMs	218	218	218	218
*SM capacitance (mF)	8	8	15	15
*Arm inductance (mH)	100	100	50	50
*Arm resistance (Ω)	1.32	1.32	0.66	0.66

Note: * indicates that considering the symmetry, parameters of positive MMC are listed.

The DC transmission line adopts the distributed FD model for precisely reflecting the EMT process [22]. The parameters of RL model based DC line are those of the FD model at 200 Hz [14]. The resistance per unit length is 0.0028 Ω/km; the self-inductance per unit length is 1.924 mH/km; and the mutual inductance per unit length is 0.996 mH/km.

As shown in Fig. 7, two negative PTG faults (F_1 and F_2) are assumed to occur in the middle of Line 24 and Line 12 at 1.5 s, respectively. The node numbers of F_1 and F_2 are 5 and 5′, respectively. The fault resistance of F_1 is set to 15 Ω, while that of F_2 is set to 0.01 Ω. Meanwhile, considering the interruption time of DCCB, the duration of Stage 1 is set to be 5 ms. During PTG fault, the DCCBs in HVDC grid are assumed not to open, which aims to see the correctness and accuracy of the PTG fault analysis at Stage 1.

A. Validation of MMC Average-value Model

A comparative study between the detailed switching model of MMC and the average value model is performed to analyze their steady state and fault transient performance. Both models adopt the parameters listed in Appendix B, Table B1. The equivalent capacitance of each arm in average value model is C/N. Figure 8 shows the comparison results.

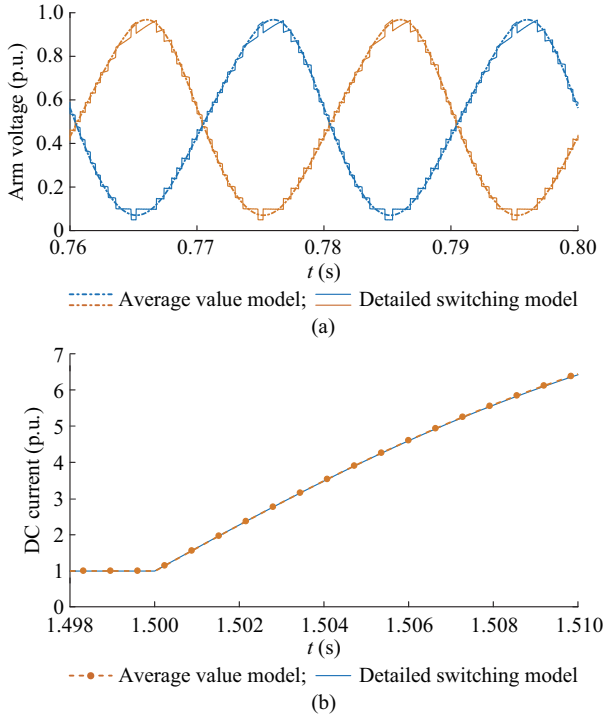


Fig. 8. Comparison between detailed switching model and average value model. (a) Arm voltage of phase A at steady state. (b) DC current during DC fault.

Figure 8(a) is the arm voltage of phase A in steady state. Compared with the detailed switching model, the average value model neglects the nearest level modulation (NLM) process. Without considering the NLM process, the performance of average value model matches well with that of the detailed switching model. Actually, if the number of SMs increases to several hundred (e.g., 200), the mismatch caused by the NLM process will be largely decreased. Figure 8(b) is the DC current during DC fault. The fault characteristics of the average value model still match well with that of the detailed switching model. Combining Fig. 8(a) and (b), it can be concluded that the average equivalence is accurate and adequate for the reason on steady-state and fault transient characteristics.

B. Comparison Between Analytical PTG Fault Characteristics and Simulation Results

The fault F_1 is taken as an example. According to the proposed analysis method, the HVDC grid is transformed into Fig. 9, which consists of fault boundary condition and CDM networks. Neglecting the resistance, the impedance matrices are written as:

$$\boldsymbol{Z}^{\Sigma} = s\begin{bmatrix} 0.20 & 0.05 & 0.08 & 0.03 & 0.04 \\ 0.05 & 0.22 & 0.03 & 0.06 & 0.14 \\ 0.08 & 0.03 & 0.19 & 0.05 & 0.04 \\ 0.03 & 0.06 & 0.05 & 0.21 & 0.13 \\ 0.04 & 0.14 & 0.04 & 0.13 & 0.35 \end{bmatrix} \tag{27}$$

$$\boldsymbol{Z}^{\Delta} = s\begin{bmatrix} 0.18 & 0.06 & 0.07 & 0.04 & 0.05 \\ 0.07 & 0.18 & 0.04 & 0.07 & 0.13 \\ 0.07 & 0.04 & 0.17 & 0.06 & 0.05 \\ 0.04 & 0.07 & 0.06 & 0.18 & 0.12 \\ 0.05 & 0.13 & 0.05 & 0.12 & 0.24 \end{bmatrix} \tag{28}$$

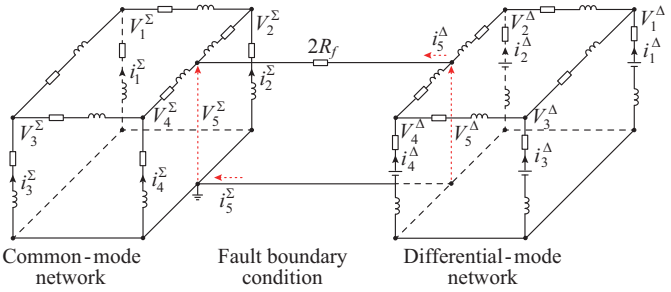


Fig. 9. Transformed CDM networks and fault boundary condition.

Substituting the impedance matrices into (13), the transfer impedances are acquired as $z_{js,1} \approx (210.12+4.13s)\,\Omega$, $z_{js,2} \approx (198.61+3.90s)\,\Omega$, $z_{js,3} \approx (87.73+1.72s)\,\Omega$, $z_{js,4} \approx (82.36+1.62s)\,\Omega$. Then, based on (15)-(19) and (21)-(24), the CDM components of PTG fault transient voltage and current are deduced. Furthermore, with inverse CDM transformation, the fault characteristics in positive and negative poles are obtained, and the validity is verified by comparison with the simulation results.

Figures 10 and 11 show the comparison of the calculated and simulated fault current and node voltage, respectively. Both simulation and calculation results are presented in per unit values, where the current base is 3 kA and the voltage base is 500 kV. In Figs. 10 and 11, transient oscillation components and their attenuation effect can be observed in the simulated fault current and voltage. The oscillation phenomena is due to the interaction between DC line inductance and stray capacitance, and the attenuation effect is determined by the DC resistance. Without consideration of the transient oscillations, the calculated curves match highly with the simulated results at Stage 1 of the protection sequence (5 ms), which verifies the validity of the proposed fault analysis method.

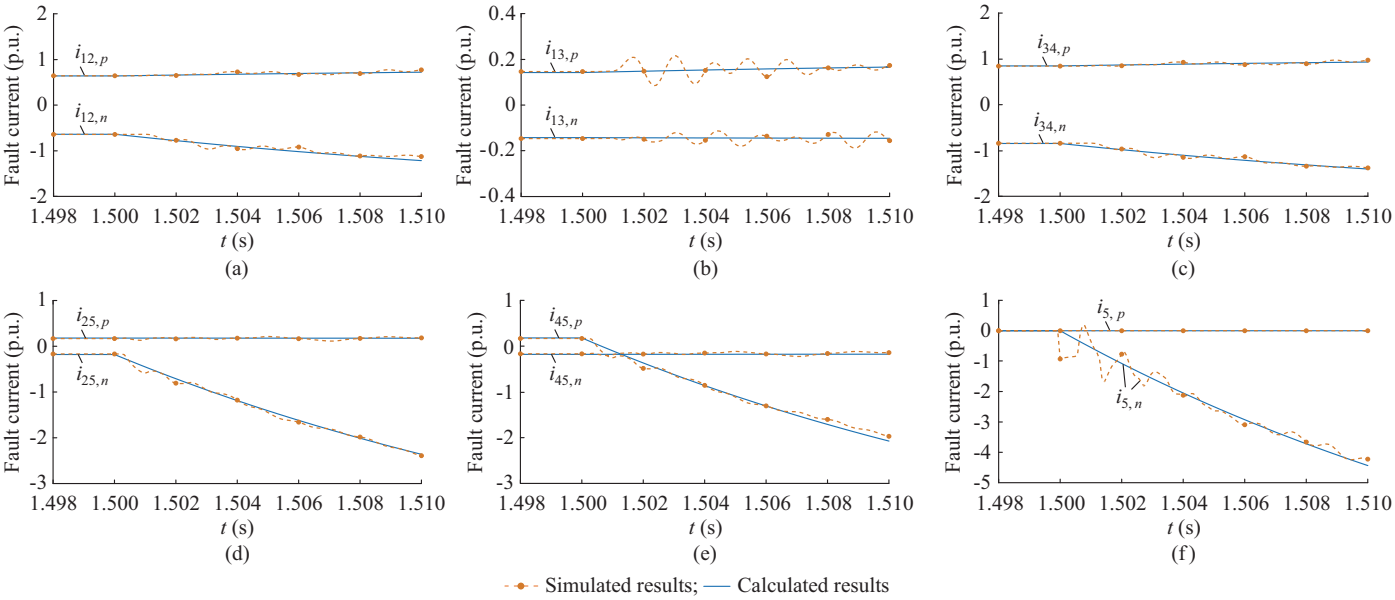


Fig. 10. Comparison of calculated fault current for fault F_1 with simulated current. (a) Branch 12. (b) Branch 13. (c) Branch 34. (d) Branch 25. (e) Branch 45. (f) Fault point.

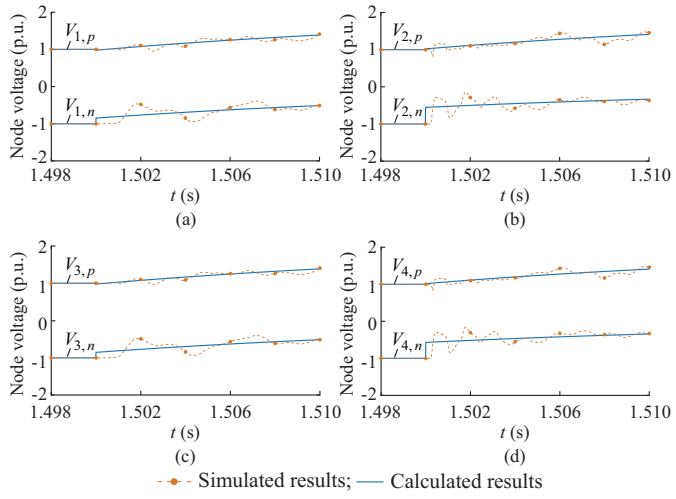


Fig. 11. Comparison of the calculated node voltage for fault F_1 with simulated results. (a) Node 1. (b) Node 2. (c) Node 3. (d) Node 4.

It should be pointed out that the transient oscillation components are associated with the frequency-dependent parameters of DC line [15], [22]. Analytical description of the oscillations is quite complicated and difficult. Although this paper does not take the oscillations into consideration, the proposed analysis can still be applied to the selection of DC equipment, which will be presented in the following section.

C. Influence of DC Inductance on Calculation Accuracy

The influence of DC inductance on the calculation accuracy is investigated. Take the fault F_1 as an example, and the fault point current $i_{5,n}$ is observed. Figure 12 shows the comparison of the calculated and simulated fault current with different neutral line reactors. It can be found that the calculation accuracy decreases with the reduction of DC line inductance (neutral line reactor). This is because the fault current rises more rapidly with a reduction of DC line inductance. Therefore, the variation of sub-module capacitor voltage exceeds 0.1 p.u., which results in an invalid DC-side equivalence of MMC station. However, the breaking capacity of DCCB is limited. As shown by the black dashed line in Fig. 12, with the reduction of DC line inductance, the duration time of Stage 1 is shortened. At Stage 1 of each scenario, the calculated results still match well with the simulation. Thus, it can be concluded that the proposed PTG fault analysis method has a satisfactory calculation accuracy with different DC line inductances.

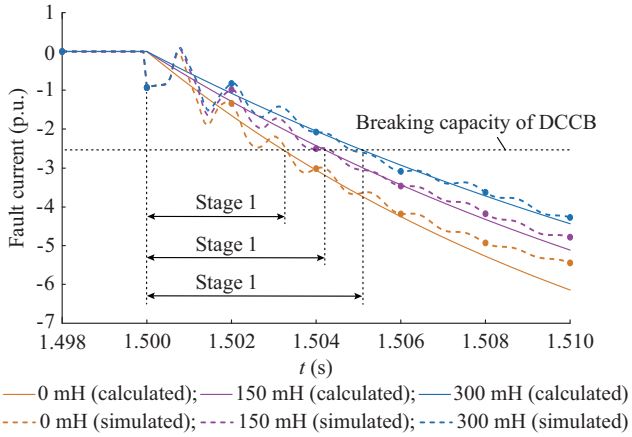


Fig. 12. Comparison of calculated and simulated fault current with different neutral line reactors.

D. Application of Proposed Fault Analysis Method

As mentioned above, the proposed fault analysis method can be used to select the DC protection equipment such as DCCBs. In this section, it is illustrated by a case.

Take the selection of DCCB at the negative pole of line 12, which is marked with red in Fig. 7, as an example. The selection procedure is presented in Fig. 13. Firstly, considering rapid dynamic performance, a relatively small DC induc-

tance (the neutral line reactor equals to 100 mH in this case) is selected. Since the DCCB should be able to isolate any negative PTG fault on line 12 within limited duration of Stage 1 (5 ms) and guarantee the continuous operation of the MMC stations, the maximum fault current $i_{15,n}$ and the maximum arm current of S1 with different fault locations on line 12 are calculated based on the proposed analysis method, respectively. Calculation results are shown in Fig. 14, where the abscissa axis means the ratio of the distance between the fault location and node 1 to the total length of line 12.

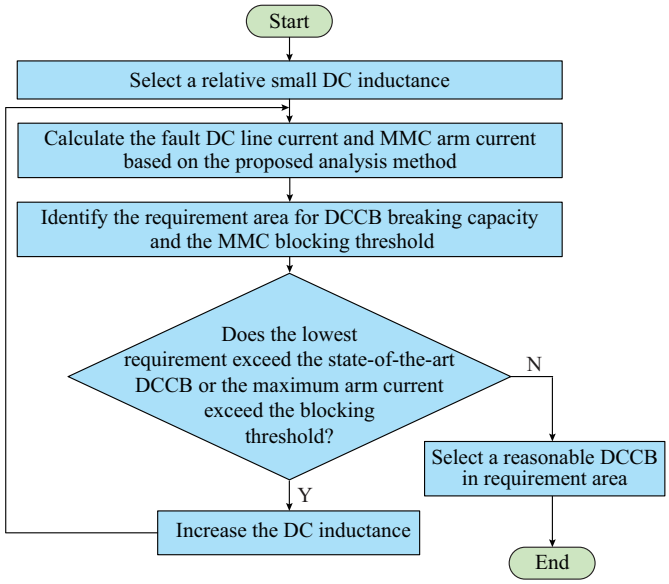


Fig. 13. Flowchart of DCCB selection.

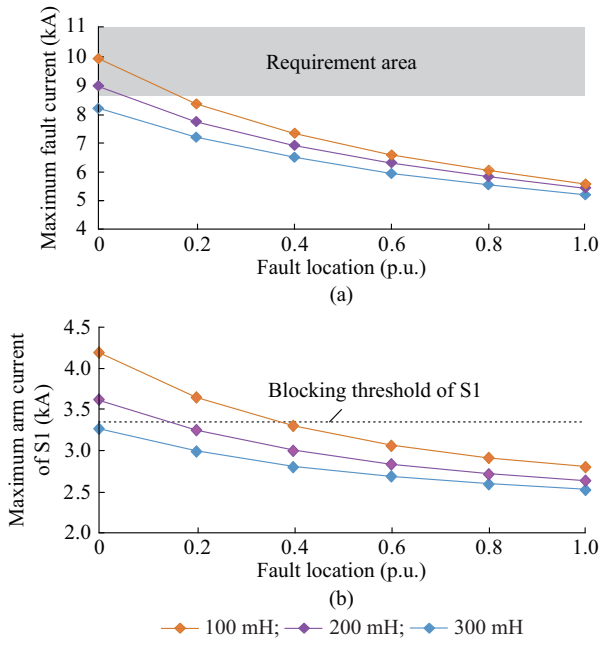


Fig. 14. Maximum fault current $i_{15,n}$ and maximum arm current of S1 with different fault locations and neutral line reactors. (a) Maximum fault current $i_{15,n}$. (b) Maximum arm current of S1.

As shown in Fig. 14(a), based on the maximum value of $i_{15,n}$ and considering the transient oscillations, the requirement area for DCCB breaking capacity, which is marked with shadow in Fig. 14(a), can be identified. Meanwhile, the blocking threshold of S1 is depicted as the dashed line in Fig. 14(b). If the lowest requirement for DCCB exceeds the state-of-the-art DCCB or the maximum arm current exceeds the blocking threshold, the DC inductance should be increased to lower the requirement, which is shown as the purple and blue lines in Fig. 14(a) and (b). The corresponding DCCB can be selected until the available DCCB can satisfy the lowest requirement and does not cause the blocking of S1.

VI. Discussion

In Section V, the proposed analysis method is applied to the selection of DCCB. In this section, other practical applications are discussed.

A. Optimal Design of DC Inductance

Both the dynamic performance and fault protection requirements need to be considered for the design of DC inductance [23]. In Section V, the fault current calculation accuracy with different DC inductances has been verified. Thus, the maximum fault current with different DC inductances can be calculated. In the scenarios with limited breaking capacity of DCCB, the calculated maximum fault current can be used to identify the limited value of DC inductance [24], which is important for the optimal design of DC inductance.

B. Parameter Setting of DC Terminal Protection Relays

It should be pointed out that the proposed analysis method is not suitable for the parameter setting of DC line protection relays, since the transient oscillations are not considered. However, it is applicable for the setting of DC terminal protection relays.

The DC terminal protection relays of MMC are mainly based on the instantaneous values of arm current and DC terminal voltage. Although the transient oscillations are not considered in the proposed analysis method, the transient oscillations would be filtered out by the DC line reactors and DC-side shunt filters [22]. Thus, the proposed fault analysis method can still be used to calculate the instantaneous values of MMC arm current and DC terminal voltage. Based on that, parameters of DC terminal protection relays can be properly set.

VII. Conclusion

This paper investigates the PTG fault characteristics in a symmetrical bipolar based MMC-HVDC grid. A CDM transformation based PTG fault analysis method is proposed. Compared with the existing work, the factors including the asymmetrical property of PTG fault, the coupling between DC transmission lines and the complexity of the structure of DC grid are all considered. Based on the analysis method, analytical expressions of the PTG fault characteristics that vary with space and time are obtained. Simulation results show that the calculated fault characteristics are accurate and can be applied to the selection of DC protection equipment.

APPENDIX A

The time constant of SM capacitor τ is defined as the ratio of the energy stored in the sub-modules (SMs) to the rated active power:

$$\tau = \frac{C_{eq}V_{dc}^2}{2V_{dc}I_{dc}} = \frac{C_{eq}V_{dc}}{2I_{dc}} \tag{A1}$$

where C_{eq} is the DC-side equivalent capacitance. The typical value of τ is around 50 ms. At Stage 1 of the fault protection sequence, the DC current variation can be approximately considered to be linear. Thus, the voltage variation of DC equivalent capacitor is expressed as:

$$\Delta V_{dc} = \frac{1}{C_{eq}}\int_0^{T_{stage1}} \Delta I_{dc}\mathrm{d}t = \frac{1}{2C_{eq}}\Delta I_{dc}T_{stage1} \tag{A2}$$

where ΔV_{dc} is the voltage variation; ΔI_{dc} is the DC current increment; and T_{stage1} is the time durations of Stage 1 (typically around 5 ms). The following are the deviations of the maximum voltage variation of MMC ΔV_{dc} in rectifier and inverter operation modes, respectively.

1) Rectifier Operation Mode

Considering only the fundamental DC frequency components, the maximum arm current of MMC during the fault can be expressed as:

$$I_{arm,\max} = I_{dc}/3 + I_m/2 + \Delta I_{dc}/3 \tag{A3}$$

where the positive direction of I_{dc} is the direction that flows out from DC terminal; and I_m is the amplitude of AC current, satisfying $0.75mI_m\cos\theta = I_{dc}$, m and θ are the modulation indexes and power factor angle, respectively. In order to maintain the continuous operation of MMC, I_{arm} is generally limited to 2 p.u. during Stage 1 [10]. Meanwhile, if the circulated current injection control is considered [25], the limitation will be stricter. Therefore, in this paper, a limitation of 1.70 p.u. is adopted. Assuming $m = 0.9$, $\cos\theta = 1$, the current increment can be estimated as:

$$\Delta I_{dc} \le 0.7I_{dc} + 1.4I_{dc}/(m\cos\theta) \approx 2.26I_{dc} \tag{A4}$$

Substituting (A1) and (A4) into (A2), we can obtain:

$$\Delta V_{dc} \le 0.06V_{dc} \tag{A5}$$

2) Inverter Operation Mode

Similarly, the maximum arm current of MMC during the fault is expressed as:

$$I_{arm,\max} = -I_{dc}/3 + I_m/2 + \Delta I_{dc}/3 \tag{A6}$$

Substitute the limitation of 1.7 p.u. into (A6), it yields:

$$\Delta I_{dc} \le 2.7I_{dc} + 1.4I_{dc}/(m\cos\theta) \approx 4.26I_{dc} \tag{A7}$$

Thus, the maximum voltage variation can be obtained:

$$\Delta V_{dc} \le 0.1V_{dc} \tag{A8}$$

Combining (A5) and (A8), it is concluded that the voltage variation of DC equivalent capacitor during Stage 1 is within 0.1 p.u..

APPENDIX B

TABLE BI
PARAMETERS OF DETAIL SWITCHING MODEL AND AVERAGE-VALUE MODEL

Parameter	Value
Rated DC voltage (kV)	500
Rated AC voltage (kV)	260
Rated DC current (kA)	1.5
Arm inductance (mH)	100
Arm resistance (Ω)	1.32
Sub-module capacitance (mF)	1
Number of sub-modules	20

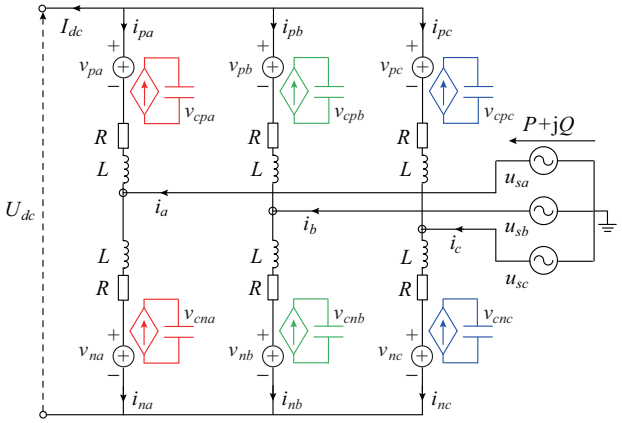


Fig. B1. Configuration of average-value model based MMC.

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