Coordination Control of Power Flow Controller and Hybrid DC Circuit Breaker in MVDC Distribution Networks

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***Abstract*—The two main challenges of medium voltage direct current (MVDC) distribution network are the flexible control of power flow (PF) and fault protection. In this paper, the power flow controller (PFC) is introduced to regulate the PF and inhibit the fault current during the DC fault. The coordination strategy of series-parallel PFC (SP-PFC) and hybrid DC circuit breaker (DCCB) is proposed. By regulating the polarity and magnitude of SP-PFC output voltage during the fault, the rising speed of fault current can be suppressed so as to reduce the breaking current of hybrid DCCB. The access mode of SP-PFC to the MVDC distribution network and its topology are analyzed, and the coordination strategy between SP-PFC and hybrid DCCB is investigated. Moreover, the emergency control and bypass control strategies of SP-PFC are developed. On this basis, the mathematical model of SP-PFC in different fault stages is derived. With the equivalent model of SP-PFC, the fault current of the MVDC distribution network can be calculated accurately. A simulation model of the MVDC distribution network containing SP-PFC is established in MATLAB/Simulink. The fault current calculation result is compared with the simulation result, and the effectiveness of the proposed coordination strategy is verified.**

***Index Terms*—Medium voltage direct current (MVDC) distribution network, fault current, power flow controller (PFC), DC circuit breaker (DCCB).**

I. Introduction

THE medium voltage direct current (MVDC) distribution network consisting of the modular multilevel converter (MMC) has various advantages such as flexibility, controllability, high power quality, and massive power transmission capacity [1], [2]. However, the MVDC distribution network is a low-inertia system. When a DC short-circuit fault occurs, MMC discharges rapidly, which leads to a rapid increase in fault current [3]. If the fault is not isolated and cleared quickly, the power electronics devices in MMC can be damaged due to the huge fault current. Additionally, the non-faulty line and MVDC distribution network will also be influenced. Therefore, suppressing the fault current and quickly clearing the fault are very critical [4].

The DC fault can be cleared quickly using a hybrid DC circuit breaker (DCCB) in MVDC distribution networks [3], [4]. However, due to the time delay of fault detection and mechanical switching action of hybrid DCCB, it takes 5-6 ms to clear the DC fault. When one severe fault occurs, the fault current may rise to a significant value so that the overcurrent protection of the MMC bridge arm is triggered. After that, the MMC is blocked, and the non-faulty line will be influenced [5]. If the fault current suppression strategy can be adopted, the rising rate of the fault current will be reduced, thereby decreasing the probability of MMC blocking. Besides, the breaking current of hybrid DCCB is also reduced. This helps lower the manufacturing cost of hybrid DCCB [6].

The current-limiting reactor (CLR) is widely used as a passive fault current-limiting device (FCLD) to suppress the rise of fault current [7]. However, the current-limiting capability of CLR is affected by the characteristics of the fault current [8]. Besides, excessive CLR parameters may affect the response speed of the control and the stability of the system [9], [10]. Therefore, other fault current inhibition methods such as active FCLDs need to be proposed. At present, active fault current inhibition methods for MVDC distribution networks can be categorized into three types: ① reducing DC bus voltage by controlling MMC blocking; ② using a dedicated DC fault current limiter (FCL); ③ introducing an active control device like PFC to output reverse voltage.

In [11], a fault isolation approach based on a bypass thyristor is proposed, where the bypass thyristor of the MMC submodule is reconfigured to form a line commutated converter (LCC). The bypass LCC can shunt the fault current and output reverse voltage to inhibit the rising speed of fault

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current. However, with this approach, a three-phase AC-side short-circuit fault happens, and it takes 15-25 ms to clear the fault, during which the AC grid will suffer high current stress. In [12] and [13], a coordination strategy between the MMC and DCCB is proposed. The MMC is blocked during the delay of DCCB mechanical switching action. However, as the voltage of the DC bus is also changed, the non-faulty line will be influenced.

Several dedicated FCLs have been proposed to solve the aforementioned shortcomings. By using a saturation effect, the reactance of an FCL can increase during the fault [6]. However, the reactance increase is finite, and thus its capability of suppressing fault current is also limited. The superconductive FCL with a similar principle has a better fault current suppression capability [14]. However, superconducting technology is far from mature and suffers from high capital expenditure and operating expense. In [15] and [16], the parameter optimization method of solid-state FCL and passive FCLD is studied, whose purpose is to reduce the cost of the equipment while reducing the fault current. However, the power losses of solid-state FCL is high during the normal operation.

Another solution is to use the existing equipment such as a DC transformer or power flow controller (PFC) in the MVDC distribution network for fault current suppression. This solution does not require any investment on hardware or affect the operation of non-faulty lines, which has certain advantages over the aforementioned solutions. The DC transformer is blocked after the fault is detected to isolate the fault side from the non-fault side [4]. However, this method cannot suppress the fault current in MMC.

In a MVDC distribution network, PFC is required to be installed to flexibly adjust the power flow (PF) of DC lines [17], [18]. According to the access mode to the MVDC distribution network, the PFC can be divided into parallel, series, and series-parallel types [19]. In [20], a fault isolation scheme based on parallel PFC is investigated, and this PFC can be equivalent to a DC transformer. The parallel PFC needs to withstand the rated voltage and current of the system. Therefore, the capital expenditure of the parallel PFC is high. In [21], a fault current inhibition method based on series PFC is proposed. However, the coordination strategy between series PFC and DCCB is not studied. Besides, the fault current calculation method of the MVDC distribution network containing series PFC is not studied. In [22], a composite topology of series PFC and DCCB is proposed. During the normal operation, the main circuit branch of DCCB is used as a series PFC. During the DC fault, this branch recovers its breaking function. However, this method makes DCCB manufacturing complicated. The series PFC relies upon the power exchange between different DC lines when regulating the PF, therefore using the series PFC may also aggravate the fluctuation of the line current.

In comparison with parallel PFC, series-parallel PFC (SP-PFC) only needs to process partial rated PF. Therefore, the SP-PFC is cost-effective [23], [24]. Furthermore, when regulating the PF, the SP-PFC does not rely on the power exchange between different DC lines. Therefore, the output voltage of SP-PFC becomes more independent. The comparison of advantages and disadvantages of different fault current suppression methods is listed in Table I. It can be concluded that the cost and power losses of SP-PFC are lower, and it also has a good fault current suppression capability. Besides, the SP-PFC has less impact on the system compared with other methods.

TABLE I
COMPARISON OF ADVANTAGES AND DISADVANTAGES OF DIFFERENT FAULT CURRENT SUPPRESSION METHODS

Method	Device	Impact on system	Suppression effect on fault current	Complexity	Cost	Power loss
Passive FCLD	CLR	Reduce response of control system	Influenced by fault current characteristics	Low	Low	Low
Active FCLD	Saturated core FCL	No impact	Limited by capacity of saturated current limiter	High	Low	Low
	Superconductive FCL	No impact	Immature technology	High	High	Low
	Solid-state FCL	No impact	High	Medium	High	High
	MMC with short blocking	Affect non-faulty lines	Medium	Low	Low	Low
	MMC with double thyristor	Cause AC three-phase short circuit	High	Medium	Low	Low
	Series PFC	Affect non-faulty lines	Medium	Low	Low	Low
	Parallel PFC	No impact	Medium	High	High	High
	SP-PFC	No impact	Medium	Low	Low	Low

In [25], a fault protection approach of an MVDC distribution network containing SP-PFC is developed. The DC fault is cleared through a solid-state DCCB, and the SP-PFC can be bypassed quickly from the DC fault. The DC fault can be cleared by the solid-state DCCB immediately after the DC fault is detected. However, the solid-state DCCB is not suitable for high voltage applications due to its high cost and the trade-off between the voltage rating and conduction loss. In the high voltage DC network, the hybrid DCCB is thus mostly adopted. The coordination between the SP-PFC and hybrid DCCB is promising in terms of cost, efficiency, and control flexibility. However, a thorough investigation of the coordination strategy is still missing.

As a result, a coordination strategy of SP-PFC and hybrid DCCB is proposed in this study. The SP-PFC is used as an FCL during the delay of the mechanical switching action of hybrid DCCB. The contributions of this study are as follows.

1) The coordination timing sequence between the SP-PFC

and hybrid DCCB is analyzed. Besides, the emergency control and bypass control strategies of SP-PFC are developed.

2) The fault calculation model of SP-PFC in different fault stages is derived, and the short-circuit current calculation method of the MVDC distribution network containing SP-PFC is presented.

3) The potentials of SP-PFC in fault current suppression and protection are released, which reduce the breaking current and investment cost of hybrid DCCB.

For enhancing the control of multi-terminal MVDC distribution networks, the SP-PFC needs to be installed. Therefore, the proposed strategy does not require additional costs. The rest of this paper is organized as follows. The access mode of SP-PFC to the MVDC distribution network and its topology are analyzed in Section II. The coordination timing sequence between the SP-PFC and hybrid DCCB is explained in Section III. The fault calculation model of SP-PFC in different fault stages is derived in Section IV. The simulation results are provided in Section V, and the conclusion is drawn in Section VI.

II. Access Mode of SP-PFC to MVDC Distribution Network and Its Topology

Figure 1(a) presents the topology of SP-PFC and hybrid DCCB [23], [24]. The SP-PFC consists of a dual active bridge (DAB) and a full-bridge converter (FBC). The high-voltage side of DAB is in parallel connection to the DC bus, and the output voltage of FBC is in a series connection to the transmission line. The primary side and secondary side of DAB are connected through an isolation transformer. The output voltage of SP-PFC varies only within a small range. Therefore, the SP-PFC only needs to process the partial power of the system. In Fig. 1(a), S_1-S_{12} are the power electronic switches of SP-PFC; I_{in} and C_{in} are the input current and capacitance of PFC, respectively; V_{dc} and C_{dc} are the output voltage and capacitance of DAB, respectively; V_1 and V_2 are the input and output voltages of the SP-PFC, respectively; L_f and C_f are the filter inductance and capacitance at the output side of the SP-PFC, respectively; V_k is the output voltage of PFC; I_L is the current of DC line; Ts1 represents the isolation transformer; K_M is the mechanical switch of the main circuit branch of hybrid DCCB; R_σ and L_σ are the leakage resistance and inductance of Ts1, respectively; and L_{sr} is the inductance of the CLR. The hybrid DCCB consists of 3 branches, namely the main circuit branch, transfer branch, and metal oxide arrester (MOA) branch. L_{sr} is installed between the SP-PFC and DC line, as shown in Fig. 1(b). When the DC fault occurs, the L_{sr} can maintain the stability of the DC bus voltage and SP-PFC output voltage.

The topology of SP-PFC accessed to the MVDC distribution network is shown in Fig. 1(b), where the HB-MMC stands for the half-bridge MMC. The HB-MMC in Fig. 1(b) is controlled with constant voltage, and the SP-PFC is installed at the exit side of the HB-MMC. The hybrid DCCB can be connected between the SP-PFC and DC line.

The configuration principles of SP-PFC and hybrid DCCB in the MVDC distribution network are as follows. For a MVDC distribution network, the hybrid DCCB should be installed in each DC line to ensure the normal operation of non-faulty lines. For the SP-PFC, its function is to increase the control freedom of the MVDC distribution network. Since each MMC station has independent voltage control capability, only one SP-PFC needs to be installed in a ring MVDC distribution network. Besides, the SP-PFC should be configured in an MMC station with constant voltage control, or it should be installed in an MMC station with the grounding point.

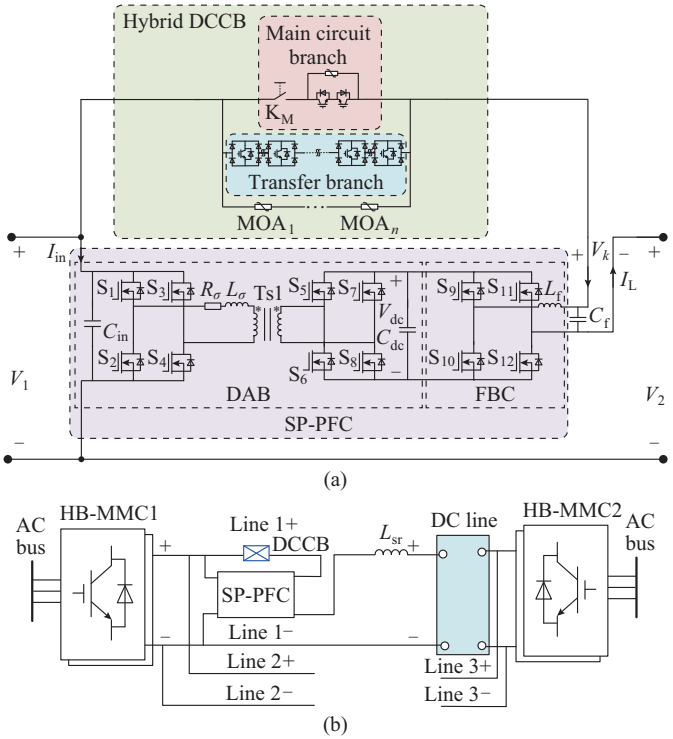


Fig. 1. Topology of SP-PFC and hybrid DCCB and topology of SP-PFC accessed to MVDC distribution network. (a) Topology of SP-PFC and hybrid DCCB. (b) Topology of SP-PFC accessed to MVDC distribution network.

III. Coordination Strategy of SP-PFC and Hybrid DCCB

A. Coordination Control of SP-PFC During DC Fault

In this paper, the control diagram of DAB is shown in Fig. 2(a), where V_{dc}^* is the reference value of V_{dc}; K_p and K_i are the proportional and integral coefficients, respectively; and d is the duty ratio of DAB. The constant voltage control is applied in DAB, which makes V_{dc} a constant.

The control diagram of FBC is shown in Fig. 2(b), where V_L and P_t are the voltage and transmitted power of the DC line, respectively; P_t^* and V_k^* are the reference values of P_t and V_k, respectively; D_{set} is the threshold of emergency control; V_{set} is the upper limit of V_k; and PWM stands for pulse width modulation. During the normal operation, the constant power control is adopted for FBC, aiming to make the power transmitted by the DC line constant. The blue and pink arrows represent the trigger conditions, and the lines with endpoint represent the switching signals. When a DC fault occurs, the emergency control is applied for FBC. The criterion is the change rate of I_L (dI_L/dt). When $dI_L/dt > D_{set}$, the

emergency control is activated. When the emergency control is activated, S_9 and S_{12} in Fig. 1(a) are switched on, and S_{10} and S_{11} are blocked. The switch code of the FBC corresponding to the emergency control is shown in Fig. 2(b).

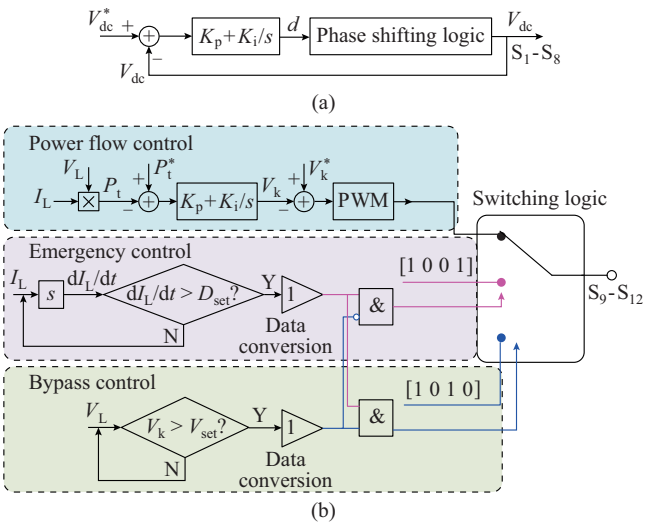


Fig. 2. Control diagrams of DAB and FBC. (a) Control diagram of DAB. (b) Control diagram of FBC.

When no intervention of the SP-PFC is required, the FBC enters the bypass control mode. When the bypass control is activated, S_9 and S_{11} in Fig. 1(a) are switched on, and S_{10} and S_{12} are blocked. Besides, when the SP-PFC is used as the FCL, the output voltage of the SP-PFC cannot exceed the withstand voltage of the FBC V_{set}. Therefore, the condition of $V_k < V_{set}$ should be satisfied during the fault. When $V_k > V_{set}$, the bypass control of SP-PFC is adopted, and the SP-PFC enters the bypass control mode. Meanwhile, the emergency control is removed.

B. Timing and Coordination Between SP-PFC and Hybrid DCCB

Figure 3 illustrates the timeline and expected time duration of the fault current suppression and protection for the SP-PFC and hybrid DCCB, where Δt_1 is the expected time duration of fault detection; Δt_2 is time interval between the fault detection and fault protection; T_{w1} is the data window of emergency control detection of SP-PFC; T_{w2} is the data window of fault protection, which includes fault detection and fault discrimination; and t_1-t_7 are the reaction time of the protection system or the switches of the hybrid DCCB. A detailed explanation is as follows.

1) Fault propagation (t_1-t_2): DC fault occurs at the beginning of this interval, then the fault current rises rapidly. The MMC and CLR discharge towards the fault point.

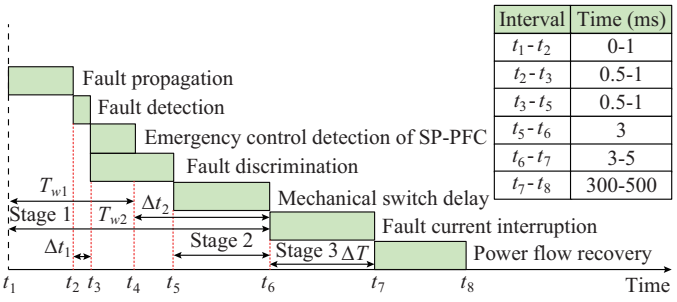
2) Fault detection (t_2-t_3): the fault in the MVDC distribution network is detected by the protection relays placed at the ends of the lines and the output side of the MMC. The protection system determines whether a fault occurs by calculating the change rate of the fault current [2]. After that, the fault protection system will start to react. The fault detection is the basis of emergency control detection and fault discrimination. Only when the fault detection conditions are satisfied, the emergency control detection and fault discrimination will be executed.

3) Emergency control detection of SP-PFC (t_2-t_4): the emergency control detection of SP-PFC and fault discrimination are carried out simultaneously. When the DC fault is confirmed, the emergency control of SP-PFC will be activated.

4) Fault discrimination (t_2-t_5): the protection system will identify whether the fault is an internal fault. After that, the faulty line is discriminated by protection relays associated to the hybrid DCCB. When the internal DC fault is confirmed, the trip signal will be sent to the hybrid DCCB.

5) Mechanical switch delay (t_5-t_6): during this interval, the hybrid DCCB commutates from the mechanical switch branch to the transfer branch. It takes a fixed delay ΔT for the mechanical switch to change from on to off state. In this study, ΔT is 3 ms. This fixed delay is conducive to SP-PFC outputting large enough reverse voltage and suppressing the fault current effectively.

6) Fault current interruption (t_6-t_7): both the mechanical switch and the transfer branch are off. The hybrid DCCB will interrupt the fault current and isolate the corresponding faulty line. Before sending the trip signal to the hybrid DCCB, the current level is checked to confirm that the SP-PFC is in the fault current suppression state, and the fault current is below the breaking capability of the hybrid DCCB.



Interval	Time (ms)
t_1-t_2	0-1
t_2-t_3	0.5-1
t_3-t_5	0.5-1
t_5-t_6	3
t_6-t_7	3-5
t_7-t_8	300-500

Fig. 3. Timeline and expected time duration of fault current suppression and protection for SP-PFC and hybrid DCCB.

C. Coordination Procedure Between Protection and Control of SP-PFC

It can be concluded from Fig. 3 that the coordination between the SP-PFC and hybrid DCCB includes two aspects: the length of the data window and the amplitude of the fault current. To enhance the ability of SP-PFC to suppress fault current, the emergency control of SP-PFC is activated earlier than the trip of hybrid DCCB. Namely, T_{w1} is set smaller than T_{w2}. Besides, the magnitude of the fault current needs to be further confirmed to ensure that the fault is internal. To meet this requirement, the magnitude of the fault current needs to exceed a fixed threshold. Before sending the trip signal to the hybrid DCCB, the magnitude of the fault current should be less than the breaking current of the hybrid DCCB. According to these principles, the coordination procedure between the SP-PFC and hybrid DCCB is shown in

Fig. 4.

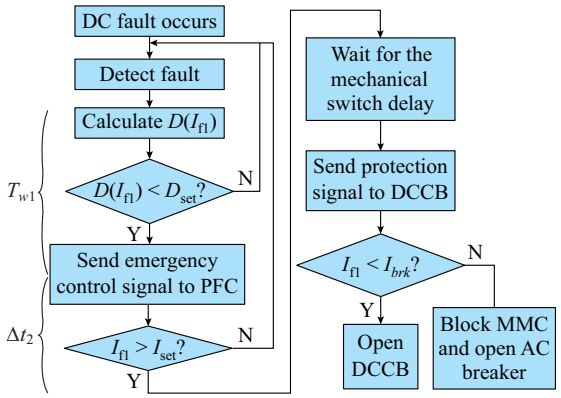


Fig. 4. Coordination procedure between SP-PFC and hybrid DCCB.

In Fig. 4, $D(I_{fl})$ is the change rate of the magnitude of fault current at HB-MMC1 side I_{fl}; I_{set} is the threshold of fault discrimination (internal fault); and I_{brk} is the breaking current of the hybrid DCCB. When a DC fault occurs, the fault detection algorithm will be executed. After that, $D(I_{fl})$ will be calculated. If $D(I_{fl}) > D_{set}$ is satisfied, the emergency control of SP-PFC will be activated. When the SP-PFC is used to suppress the fault current, the magnitude of fault current I_{fl} will be reduced. Subsequently, the magnitude of the fault current will be further confirmed. If $I_{fl} > I_{set}$ is satisfied, the fault protection signal will be sent to the corresponding hybrid DCCB. If $I_{fl} < I_{set}$, the protection system will return to the fault detection. During this procedure, the data window of the fault protection satisfies $T_{w2} = T_{w1} + \Delta t_2$.

After a delay of the mechanical switch ΔT, the trip signal will be sent to the corresponding hybrid DCCB. In order to ensure that the hybrid DCCB reliably interrupts the fault current, the fault current level and the limiting state of SP-PFC will be further checked. If $I_{fl} < I_{brk}$, the transfer branch of the hybrid DCCB will be off, and the MOA branch will be on. Otherwise, the MMC will be blocked to further suppress the fault current.

IV. Fault Calculation Model of SP-PFC in Different Fault Stages

A. Fault Calculation Model of SP-PFC in Stage 1

When a fault occurs, the MMC can be equivalent to an RLC discharging circuit [2]. The control method of SP-PFC and the timing between the SP-PFC and hybrid DCCB are consistent with Fig. 3. Therefore, the fault current expressions in different fault stages can be derived accordingly. The purposes of fault current calculation are as follows.

1) Analyze the maximum and minimum values of the fault current of the MVDC distribution network containing SP-PFC. This provides a foundation for the design of the protection threshold.

2) Evaluate the breaking current of hybrid DCCB with different fault parameters. If the fault current is larger than the breaking current of hybrid DCCB, the parameters of CLR and the maximum reverse voltage of SP-PFC should be re-selected.

3) Evaluate the fault current suppression effect of SP-PFC under different C_f, which will affect the increasing speed of V_k. Therefore, the fault current analysis under different C_f provides a perspective for the design of C_f.

In Fig. 1(b), the HB-MMC1 and HB-MMC2 represent the sending end and receiving end, respectively. Assume that the fault occurs at the exit side of HB-MMC1, and the fault transition resistance is 0. In stage 1, the input power of SP-PFC is equal to the output power. According to Fig. 1(b), V_k satisfies:

$$\begin{cases} I_{in}(u_{c1} + I_{in}R_\sigma) = V_k I_{fl} \\ I_{fl} = nI_{in} \end{cases} \tag{2}$$

where u_{c1} is the equivalent voltage at DC side of HB-MMC1; R_σ is the leakage reactance of Ts1; and n is the ratio of Ts1. As the power loss of SP-PFC is very small relative to the rated power, it is neglected in (2). As the fault detection time is within 0.5-1.0 ms, the fault current is relatively small. The SP-PFC in this stage can be equivalent to a voltage source V_k. The expressions of V_k can be obtained through (2), which satisfies:

$$V_k = \frac{u_{c1}}{n} + \frac{I_{fl}R_\sigma}{n^2} \tag{3}$$

The equivalent circuit of SP-PFC in stage 1 is shown in Fig. 5, where u_k is the transient value of V_k; R_L and L_{dc} are the equivalent resistance and inductance of the DC line, respectively; x is the ratio of the distance between fault point and HB-MMC1 to the total line length; R_f is fault transition resistance; I_{f2} is the magnitude of the fault current at HB-MMC2 side; C_{eq}, R_{eq}, and L_{eq} are the equivalent capacitance, resistance, and inductance of the MMC, respectively; and u_{c2} is the equivalent voltage at the DC side of HB-MMC2. Loops 1 and 2 are the two main fault loops.

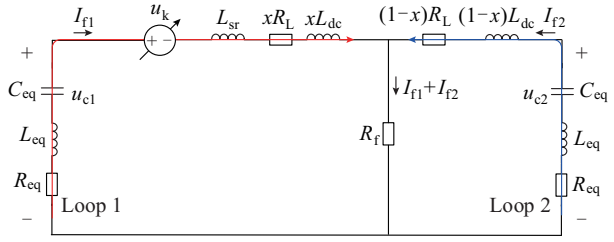


Fig. 5. Equivalent circuit of SP-PFC in stage 1.

According to the KVL of Fig. 5, the voltage and current of loop 1 satisfy:

$$\begin{cases} -u_{c1} + u_k + L_{\Sigma 1}\dfrac{\mathrm{d}i_{f1}}{\mathrm{d}t} + R_{\Sigma 1}i_{f1} + R_f i_{f2} = 0 \\ i_{f1} = C_{eq}\dfrac{\mathrm{d}u_{c1}}{\mathrm{d}t} \\ L_{\Sigma 1} = L_{eq} + L_{sr} + xL_{dc} \\ R_{\Sigma 1} = xR_L + R_{eq} + R_f \end{cases} \tag{4}$$

where i_{f1} and i_{f2} are the transient values of I_{f1} and I_{f2}, respectively.

The voltage and current of loop 2 satisfy:

$$\begin{cases} -u_{c2}+L_{\Sigma 2}\dfrac{\mathrm{d}i_{f2}}{\mathrm{d}t}+R_{\Sigma 2}i_{f2}+R_{f}i_{f1}=0 \\ i_{f2}=C_{eq}\dfrac{\mathrm{d}u_{c2}}{\mathrm{d}t} \\ L_{\Sigma 2}=L_{eq}+L_{sr}+(1-x)L_{dc} \\ R_{\Sigma 2}=(1-x)R_{L}+R_{eq}+R_{f} \end{cases} \tag{5}$$

It can be known from (3) that the I_{f1} is related to V_k. The polarity of V_k will be reversed relative to u_{c1}. According to (5), as no PFC is installed at the HB-MMC2 side, I_{f2} is determined by the fault position, fault transition resistance, the capacitance of submodule C_{SM}, and L_{sr}. However, as the HB-MMC2 needs to complete the reversion of PF in the stage 1, its fault current is relatively small.

B. Fault Calculation Model of SP-PFC in Stage 2

In stage 2, the emergency control of SP-PFC is activated. According to the current flow path, the equivalent circuit of SP-PFC in stage 2 can be obtained, as shown in Fig. 6(a). Herein, the internal dynamics inside the DAB are considered. However, this aggravates the analytical difficulty of fault current. Since C_{dc} is generally much larger than C_f, the output voltage of DAB can be equivalent to the secondary-side voltage u_{T2} of the isolation transformer. Therefore, the equivalent circuit in Fig. 6(a) can be simplified as Fig. 6(b), where loops 1-3 are the three main fault loops. The fault currents in different loops are derived, respectively.

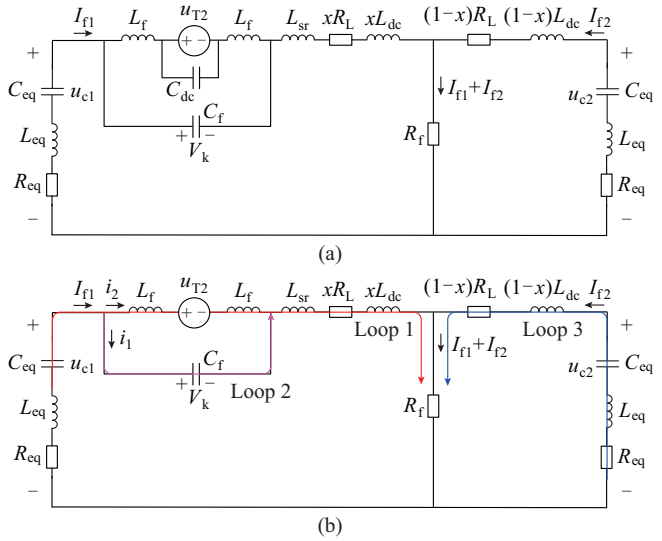


Fig. 6. Equivalent circuit and simplified circuit of SP-PFC in stage 2. (a) Equivalent circuit. (b) Simplified circuit.

As shown in Fig. 6(b), I_{f1} can be divided into i_1 and i_2. i_1 is the current following through C_f, and i_2 is the current following the secondary side of DAB. According to the KVL of loop 1, the fault current satisfies:

$$-u_{c1}+u_{k}+L_{\Sigma 1}\frac{\mathrm{d}i_{f1}}{\mathrm{d}t}+R_{\Sigma 1}i_{f1}+R_{f}(i_1+i_2+i_{f2})=0 \tag{6}$$

The KVL of loop 2 satisfies:

$$2L_{f}\frac{\mathrm{d}i_2}{\mathrm{d}t}+u_{T2}=u_{k} \tag{7}$$

i_1 and i_2 can be calculated through (6) and (7), respectively. Therefore, the fault current from HB-MMC1 I_{f1} can be calculated accordingly as $I_{f1}=i_1+i_2$. The KVL of loop 3 satisfies:

$$-u_{c2}+L_{\Sigma 2}\frac{\mathrm{d}i_{f2}}{\mathrm{d}t}+R_{\Sigma 2}i_{f2}+R_{f}(i_1+i_2+i_{f2})=0 \tag{8}$$

The current following through C_{eq} and C_f satisfy:

$$\begin{cases} i_1+i_2=i_{f1}=C_{eq}\dfrac{\mathrm{d}u_{c1}}{\mathrm{d}t} \\ i_{f2}=C_{eq}\dfrac{\mathrm{d}u_{c2}}{\mathrm{d}t} \\ i_1=C_{f}\dfrac{\mathrm{d}u_{k}}{\mathrm{d}t} \end{cases} \tag{9}$$

According to (1)-(9), the fault current of MVDC distribution network containing SP-PFC in stages 1 and 2 can be calculated.

C. Coordination of CLR and SP-PFC to Suppress Fault Current

When a DC fault occurs, the fault current is mainly inhibited by the CLR in stage 1. The effect of CLR on suppressing the fault current depends on $\mathrm{d}I_L/\mathrm{d}t$. Therefore, the CLR has the best effect of suppressing the fault current in stage 1. However, as the time duration of the fault increases, $\mathrm{d}I_L/\mathrm{d}t$ will gradually decrease. This means that the CLR may not be able to meet the requirements of fault current suppression in different stages. To observe the effect of CLR on suppressing the fault current, the parameters of the studied system are given as follows: the DC bus voltage is 100 kV, and the rated line current is 2 kA. The inductance of CLR L_{sr} is changed from 0 mH to 30 mH. The fault occurs at the exit side of HB-MMC1, and the fault transition resistance is 0 Ω. The parameters of MMC are listed as follows: the number of submodules at the input side of the MMC bridge arm $N=50$, the resistance of the MMC bridge arm $R_m=0.2$ Ω, the inductance of the MMC bridge arm $L_m=10$ mH, the capacitance of the submodule $C_{sm}=0.7$ mF, and $x=0\%$.

Figure 7(a) and (b) illustrates the fault current in the cases without and with the SP-PFC, respectively.

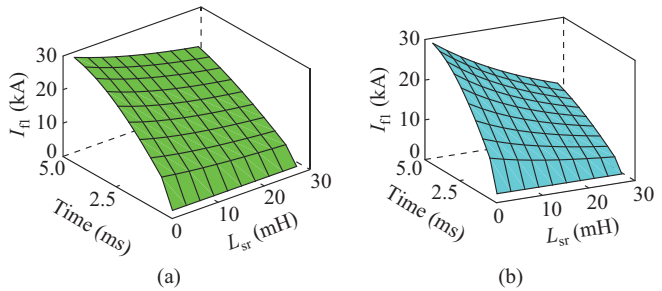


Fig. 7. Fault current under cases without and with SP-PFC. (a) Case without SP-PFC. (b) Case with SP-PFC.

Besides, the influences of L_{sr} and fault time on I_{f1} are investigated. Herein, the SP-PFC is regarded as a voltage source V_k, and V_k is a constant (10 kV). As shown in the figure, if there is no SP-PFC at the DC side, the maximum value

of I_{fl} can reach above 18 kA (t_f = 4 ms). Besides, when L_{sr} is small, the fault current may reach above 25 kA. Therefore, other fault current suppression measures need to be introduced to further reduce the breaking current of the hybrid DCCB.

In Fig. 7(b), the SP-PFC is introduced to suppress the fault current. After the SP-PFC is adopted, it can output reverse voltage to inhibit the fault current. It can be observed from Fig. 7(b) that the fault current can be suppressed below 15 kA. Therefore, when the SP-PFC and CLR are used to suppress the fault current, the breaking current of the hybrid DCCB can be reduced effectively.

D. Influence of Fault Parameters on SP-PFC

With the fault calculation model in this subsection, the influence of different fault parameters on I_{fl} and V_k can be analyzed theoretically. Figure 8(a) illustrates the I_{fl} and V_k under different transition resistances. As the transition resistance increases, the maximum amplitude of the fault current decreases. However, the maximum amplitude of V_k in Fig. 8(b) is hardly affected by the transition resistance. Therefore, the transition resistance has little effect on V_k.

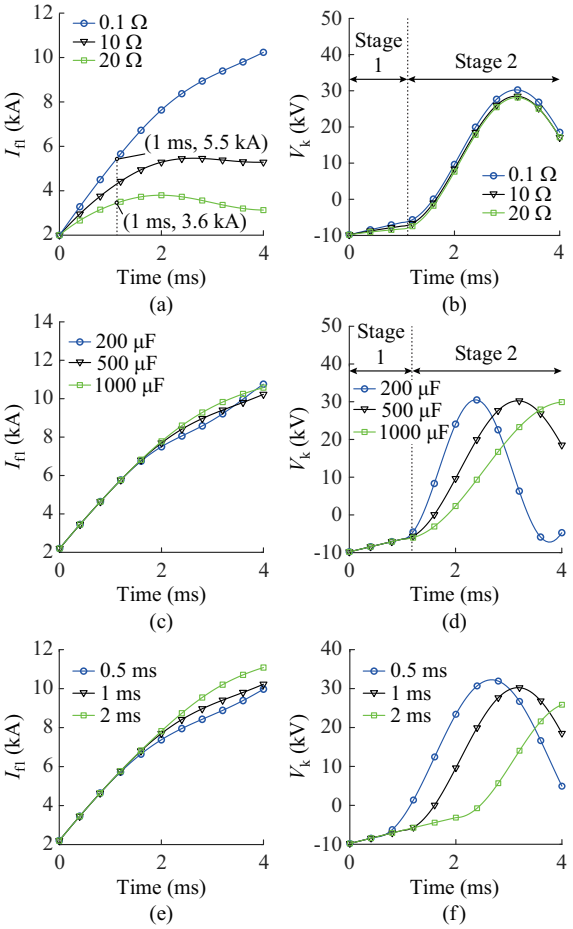


Fig. 8. I_{fl} and V_k under different fault parameters. (a) I_{fl} under different transition resistances. (b) V_k under different transition resistances. (c) I_{fl} under different C_f. (d) V_k under different C_f. (e) I_{fl} under different T_{w1}. (f) V_k under different T_{w1}.

According to the equivalent circuit of SP-PFC in stage 2, the C_f will affect the increasing speed of V_k. Therefore, C_f may have an impact on the fault current suppression effect of SP-PFC. Figure 8(c) and (d) illustrates the I_{fl} and V_k under different C_f, respectively. It can be observed that when C_f = 500 μF, the amplitude of the fault current has the minimum value. Therefore, C_f can be optimized according to the theoretical analysis in Section III. The fault current of different C_f is calculated and compared, and the optimal C_f is around 500 μF. Therefore, in the simulation, C_f is determined as 500 μF.

The length of emergency control detection window T_{w1} may also affect the magnitude of fault current. Figure 8(e) and (f) illustrates the I_{fl} and V_k with different T_{w1}, respectively. It can be observed that the smaller the T_{w1}, the smaller the magnitude of fault current. Therefore, T_{w1} can be set smaller than T_{w2} to enhance the ability of SP-PFC to suppress the fault current. This conclusion is consistent with the previous analysis.

The ability of SP-PFC to suppress fault current is related to its capacity. In practice, the capacity of SP-PFC is mainly determined by the output voltage of SP-PFC V_k. Figure 9 shows the amplitude of the fault current under different T_{w1} and V_k. It can be observed that the larger the output voltage of SP-PFC, the better the suppression effect of the fault current. However, the larger V_k means the higher the cost of SP-PFC. Therefore, the maximum output voltage of SP-PFC is designed to be 30 kV in this study, which is only equivalent to 30% of the rated voltage of the system. The size of the output filter capacitor of SP-PFC also affects its capacity, which has been discussed above. Based on the above analysis, it can be concluded that the SP-PFC can effectively suppress the fault current under small capacity and power loss, which has obvious advantages compared with the parallel PFC.

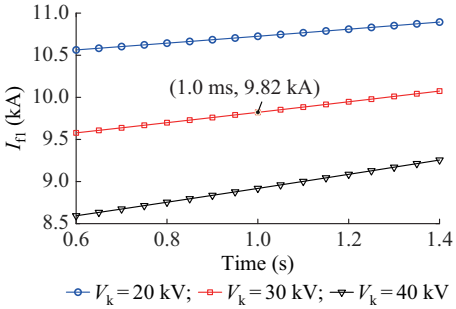


Fig. 9. Amplitude of fault current with different T_{w1} and V_k.

V. Simulation and Verification

To verify the effectiveness of the fault calculation model of SP-PFC and evaluate the suppression effect of SP-PFC on the fault current, a simulation model of MVDC distribution network shown in Fig. 10 is established in MATLAB/Simulink. Herein, MMC2 and MMC3 control the active and reactive power, where the reference values of active power of MMC2 and MMC3 are −110 MW and −220 MW, respectively, and the reference values of active power of MMC2 and MMC3 are 0 MW. MMC1 controls the DC voltage (100 kV) and reactive power (0 MW). The lumped parameter model of the transmission line and the average model of MMC are adopted. The parameters of MMC1-MMC3 are shown in Table II.

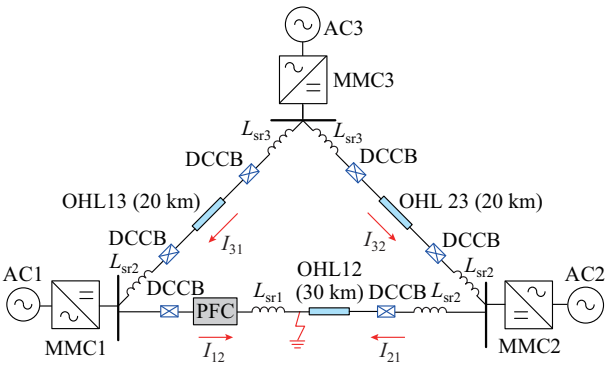


Fig. 10. Structure of simulation model of MVDC distribution network.

TABLE II
PARAMETERS OF MMC1-MMC3

Parameter	MMC1	MMC2	MMC3
Rated DC voltage (kV)	100	100	100
Rated AC voltage (kV)	66	66	66
Transformer leakage reactance (p.u)	0.15	0.15	0.15
Ratio of transformer	400 kV/ 66 kV	66 kV/ 18 kV	66 kV/ 18 kV
Bridge arm resistance (Ω)	0.01	0.01	0.01
Bridge arm inductance (mH)	15	15	15
Submodule capacitance (mF)	10	10	10
Number of submodules	50	50	50

The parameters of overhead transmission line (OHL) are as follows: $r_0 = 0.01$ Ω/km, $l_0 = 0.82$ mH/km, and $c_0 = 0.063$ μF/km. r_0, l_0, and c_0 are the resistance, inductance, and capacitance per unit length of the OHL, respectively. L_{sr1}, L_{sr2}, and L_{sr3} are the CLRs placed on the MMC1, MMC2, and MMC3 terminals, respectively. Their values are 20 mH, 10 mH, and 10 mH, respectively. The PF and current directions from the DC bus injected into the OHL are defined as positive.

To simplify the analysis, both T_{w1} and T_{w2} are set to be 1 ms. Therefore, $\Delta t_1 = 1$ ms, $\Delta t_2 = 0$ ms. The sampling frequency is selected as 20 kHz. The delay of K_M is 3 ms. Therefore, the current at 4 ms after the fault can be regarded as the breaking current of DCCB. The thresholds for different fault types are as follows. The threshold of emergency control detection D_{set} is 0.5 kA/ms. The threshold of internal fault detection I_{set} is 3 kA. The breaking current of DCCB is 15 kA. The parameters of SP-PFC are listed in Table III. The control parameters of DAB and FBC will be introduced in the following.

TABLE III
PARAMETERS OF SP-PFC

Parameter	Value
Filter capacitor of SP-PFC C_f	500 μF
Leakage inductance of isolation transformer L_σ	11 mH
Leakage resistance of isolation transformer R_σ	1 Ω
Reference of transmitted power P_t^*	220 MW
Reference of DAB output voltage V_{dc}^*	10 kV
Upper limit of output voltage of PFC V_{set}	30 kV

A. Control Parameter Design of SP-PFC

The averaged small-signal models derived in [23] are used to design the closed-loop controllers for SP-PFC. Figure 11(a) and (b) shows the open-loop transfer functions of DAB and FBC ($G_{11}(s)$ and $G_{22}(s)$), respectively. As shown in Fig. 11(a), DAB has one significant pole, which is dominated by the output capacitance. The fact that DAB has only one significant pole means that a proportional-integral (PI) controller is a good candidate for the control of V_{dc}. The PI controller functions of DAB and FBC ($G_{c1}(s)$ and $G_{c2}(s)$) can be expressed as:

$$\begin{cases} G_{c1}(s) = k_{p1} + \dfrac{k_{i1}}{s} \\ G_{c2}(s) = k_{p2} + \dfrac{k_{i2}}{s} \end{cases} \tag{10}$$

where k_{p1} and k_{i1} are the proportional and integral parameters of the DAB, respectively; and k_{p2} and k_{i2} are the proportional and integral parameters of the FBC, respectively.

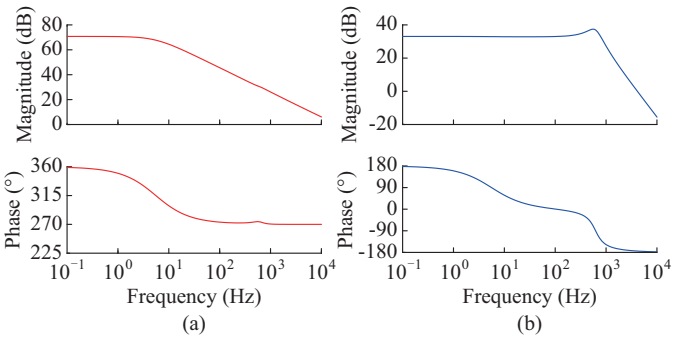


Fig. 11. Bode diagrams of open-loop transfer functions of DAB and FBC. (a) $G_{11}(s)$. (b) $G_{22}(s)$.

According to the characteristics of $G_{11}(s)$, the PI controller parameters of DAB can be designed according to [23]. The design procedure in [23] can be simplified and the proportional gain k_{p1} can be written as:

$$k_{p1} = \frac{f_c \varsigma}{2\pi f_o} \tag{11}$$

where ς is the damping coefficient and typically is set to be $1/\sqrt{2}$; f_o is the natural system frequency; and f_c is the corner frequency of $G_{11}(s)$. The corner frequency can be found in the point for which the magnitude falls by −3 dB. The integral gain k_{i1} is:

$$k_{i1} = \frac{1}{\pi f_o}\left(\frac{\pi}{2} f_c\right)^2 \tag{12}$$

According to the characteristics of $G_{22}(s)$, the PI controller parameters of FBC can be designed according to [26]. Finally, the corresponding parameters of $G_{c1}(s)$ and $G_{c2}(s)$ are $k_{p1} = 0.0038$, $k_{p2} = 0.0097$, $k_{i1} = 2.2489$, $k_{i2} = 37.9311$. The bode diagram of closed-loop transfer functions of DAB and FBC are shown in Fig. 12. The bandwidth of FBC can be much larger than DAB, which helps FBC faster respond to the changes in the fault current.

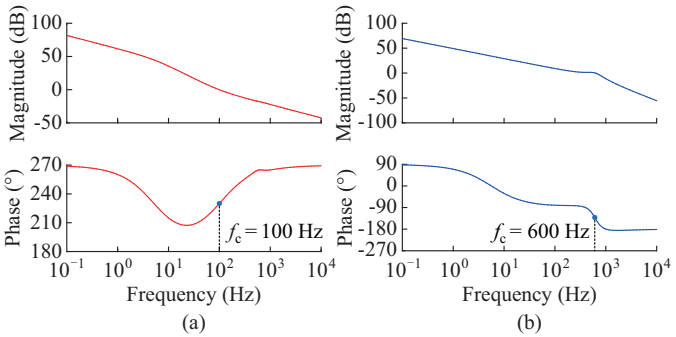


Fig. 12. Bode diagrams of closed-loop transfer functions of DAB and FBC. (a) $G_{11}(s)G_{c1}(s)$. (b) $G_{22}(s)G_{c2}(s)$.

B. Verification of Fault Calculation Model of SP-PFC

In this subsection, the validity of the fault calculation model will be verified. To maintain the consistency with the theoretical analysis, the MMC3 is removed in this simulation. The fault currents in different cases are analyzed as follows.

1) Case 1: the SP-PFC is not installed at the DC side.

A DC fault occurs at the exit side of MMC1 at 0.8 s. The fault transition resistance R_f is 0 Ω. In this case, the SP-PFC is not added to the MVDC distribution network. The corresponding fault current and DC bus voltage are shown in Fig. 13(a) and (b), respectively. It can be observed from Fig. 13(a) that the peak value of I_{fl} is 12 kA at 4 ms. In addition, the simulation result is close to the calculation result. Therefore, the equivalent model of MMC is correct. In Fig. 13(b), the voltage drop at the rectifier side is about 35 kV, which is consistent with the previous analysis.

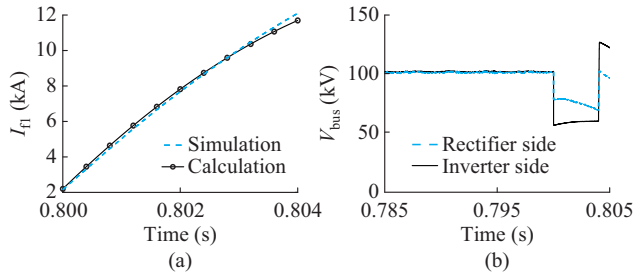


Fig. 13. Fault current and DC bus voltage without SP-PFC. (a) Simulation and calculation results of fault current. (b) Simulation results of DC bus voltage at rectifier and inverter sides.

2) Case 2: the SP-PFC is installed at the DC side. After the fault is detected, the emergency control of SP-PFC is activated.

The DC fault occurs at 0.8 s, and the fault location is at the exit side of SP-PFC. R_f is 0 Ω. Both the simulation and calculation results are shown in Fig. 14, where I_{fl} and V_k in stage 1 and stage 2 are calculated by (4) and (6)-(9), respectively. It can be observed from Fig. 14(a) that the simulation result is close to the calculation result. Therefore, the equivalent modeling method of SP-PFC in Section II is correct. Furthermore, I_{fl} is 10 kA at 0.804 s, which is reduced by 20% in comparison with Case 1. Therefore, after the emergency control of SP-PFC is adopted, the SP-PFC can effectively inhibit the fault current.

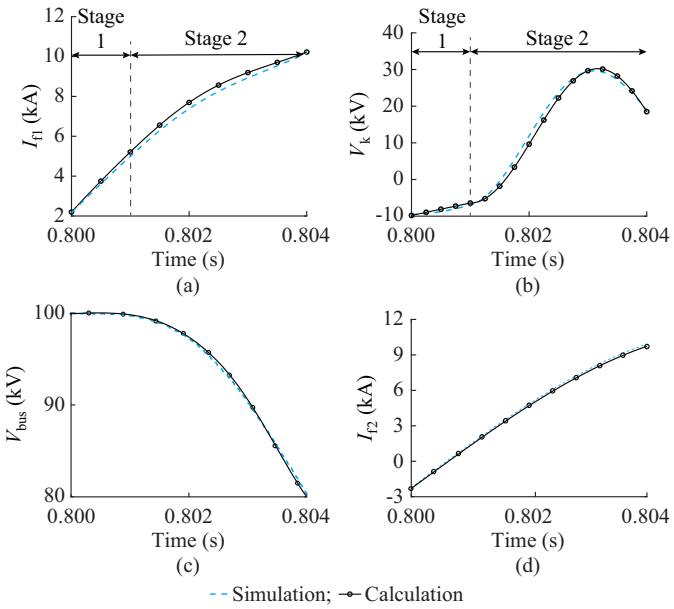


Fig. 14. Comparison of simulation and calculation results of SP-PFC with emergency control. (a) Fault current I_{fl}. (b) Output voltage of SP-PFC V_k. (c) DC bus voltage V_{bus}. (d) Fault current at inverter side I_{f2}.

From Fig. 14(b), it can be observed that the magnitude of V_k decreases slowly from −10 kV. When the fault is detected at 0.801 s, the emergency control is activated. Subsequently, V_k increases rapidly, and the polarity is changed. This is because after the emergency control is activated, part of the I_{fl} is stored in C_{dc}, and the other part is stored in C_f. Since C_f is relatively small, V_k increases rapidly. Therefore, the emergency control increases the ability of SP-PFC to suppress the fault current. V_k reaches the peak value at 0.803 s. As the peak value of V_k does not exceed 30 kV, the bypass control of SP-PFC is not triggered.

It can be observed from Fig. 14(c) that when the SP-PFC is added to the DC side of MMC, the voltage drop does not exceed 25 kV. Herein, the fault transition resistance is 0.1 Ω, and the fault location is x = 0%. In contrast, when there is no SP-PFC, the voltage drop will be greater than 35 kV, as shown in Fig. 13(b).

In addition, the output voltage of DAB V_{dc} is usually set to be 10%-30% of the DC bus voltage (10-30 kV). Therefore, the impact of the DC bus voltage drop on V_{dc} is within a controllable range, which allows the SP-PFC to provide the extra voltage for suppressing the fault current. Figure 14(c) and (d) also shows that the calculation and simulation results of the DC bus voltage and the fault current at the inverter side are very similar. This further proves that the derived fault calculation model is correct.

Figure 15(a) illustrates the calculation and simulation results of output voltage of DAB V_{dc}. It can be observed that V_{dc} remains constant in stage 1, while V_{dc} fluctuates in a small range in stage 2, which is consistent with the previous analysis. Figure 15(b) illustrates the results of u_{T1} and u_{T2}, where u_{T1} is the primary side voltages of the isolation transformer. As the DC bus voltage drops, u_{T1} drops slowly. However, u_{T2} remains almost constant. Therefore, it is reasonable to assume that the u_{T2} is constant in Section IV.

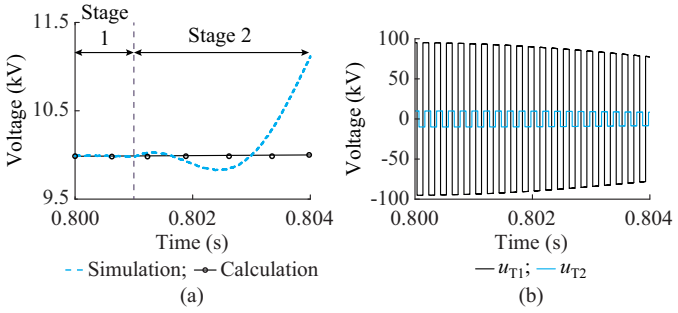


Fig. 15. Results of V_{dc}, u_{T1}, and u_{T2}. (a) V_{dc}. (b) u_{T1} and u_{T2}.

Figure 16 illustrates the comparison of fault currents (I_{f1} and I_{f2}) under lumped and distributed parameters. It can be observed that the distributed parameter increases the fluctuation of the fault current, but the corresponding fault current is very close to the fault current under the lumped parameter. Therefore, the derived fault current expression can also reflect the magnitude of the fault current with distributed parameter.

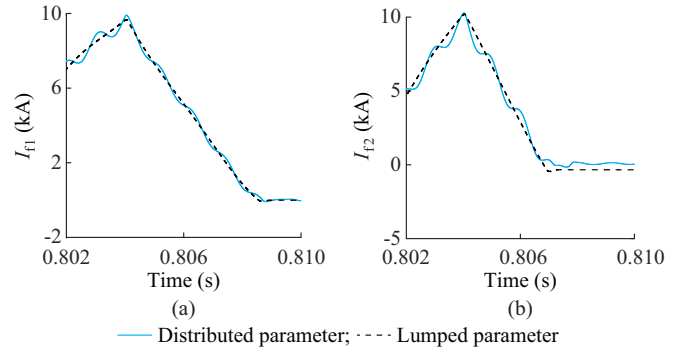


Fig. 16. Comparison of fault current with lumped and distributed parameters. (a) I_{f1}. (b) I_{f2}.

C. Influence of Different Fault Parameters

Figure 17 illustrates the simulation results under different fault transition resistances. The fault transition resistance varies from 0.1 Ω to 20 Ω. The other parameters are consistent with the Section V-B. It can be observed from Fig. 17(a) that the fault transition resistance has a significant influence on the fault current. However, the fault transition resistance has little effect on the output voltage of SP-PFC V_k. Therefore, the impact of SP-PFC on suppressing the fault current will not be affected by the fault transition resistance. Besides, the waveforms of I_{f1} and V_k are consistent with the theoretical analysis.

It can be observed from Fig. 17(c) that V_{dc} remains constant in stage 1. In stage 2, V_{dc} fluctuates slightly at the beginning and then starts to increase. In stage 3, V_{dc} increases above 12 kV when R_f is 0.1 Ω. In addition, the fault transition resistance has a significant impact on V_{dc}. However, due to the MMC is not blocked, V_{dc} will not drop to 0. From the theoretical analysis and simulation results, when an appropriate CLR is configured, the voltage drop of V_{dc} will not exceed 25% of the rated voltage.

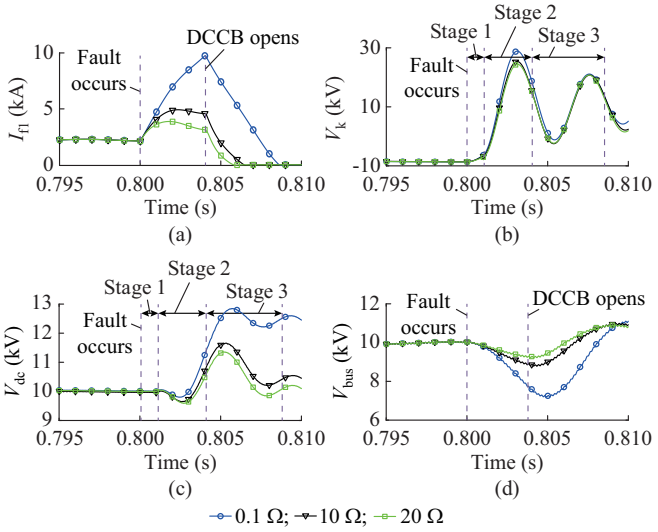


Fig. 17. Simulation results under different fault transition resistances. (a) I_{f1}. (b) V_k. (c) V_{dc}. (d) V_{bus}.

Figure 18 illustrates the simulation results with different C_f. C_f varies from 200 μF to 1000 μF. The fault transition resistance is set to be 0.1 Ω. It can be observed from Fig. 18(a) that when $C_f = 500$ μF, the breaking current of DCCB I_{f1} has the smallest value. According to the waveform of V_k, it can be observed that the integral of V_k to the time is the largest at $C_f = 500$ μF. Therefore, when $C_f = 500$ μF, the SP-PFC has the strongest ability to suppress the fault current. It can be observed from Fig. 18(c) and (d) that C_f has little impact on V_{dc} and V_{bus}. Besides, the waveforms of I_{f1}, V_k, and V_{bus} are consistent with the previous analysis.

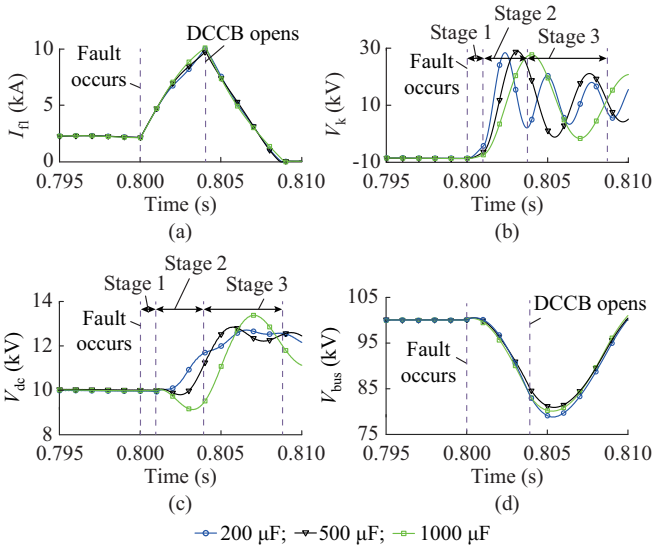


Fig. 18. Simulation results with different C_f. (a) I_{f1}. (b) V_k. (c) V_{dc}. (d) V_{bus}.

Figure 19 illustrates the simulation results with different T_{w1}. T_{w1} varies from 0.5 ms to 2 ms. It can be observed that the smaller the T_{w1}, the smaller the fault current. This conclusion is consistent with the previous analysis. Therefore, T_{w1} can be set smaller in practice to further reduce the breaking current of the DCCB. It can be observed from Fig. 19(b)

that T_{w1} has little impact on V_{dc} and V_{bus}. Besides, the waveforms of I_{fl}, V_k, and V_{bus} are consistent with the previous analysis.

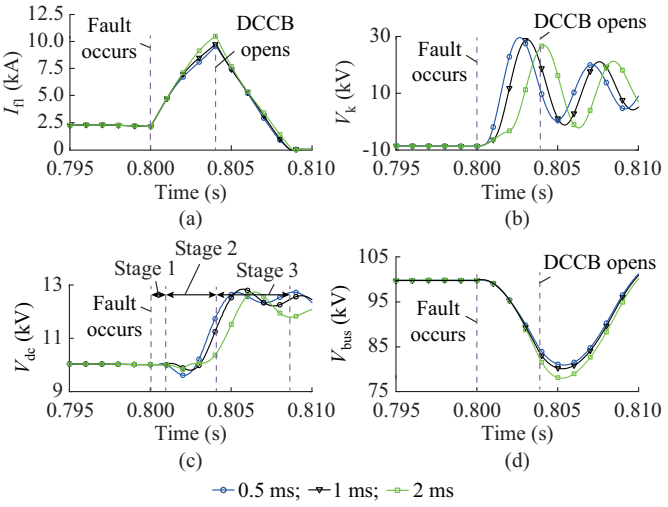


Fig. 19. Simulation results with different T_{w1}. (a) I_{fl}. (b) V_k. (c) V_{dc}. (d) V_{bus}.

VI. Conclusion

The SP-PFC is mainly used for PF control. To release its potential on fault protection, a coordination strategy of SP-PFC and hybrid DCCB is proposed. The fault protection procedure is divided into three stages, and the circuit model of SP-PFC in each stage is developed. Based on the models, the fault current of the MVDC distribution network containing the SP-PFC can be analytically calculated. Once the fault is detected, the proposed emergency control of SP-PFC will be activated to generate a reverse voltage and then slow down the rising of the fault current. The simulation results show that with the proposed emergency control, the SP-PFC can suppress the fault current by 20%. The calculation results of the fault current also matches the simulation results very well. This study also studies the timing coordination strategy of SP-PFC and hybrid DCCB. This coordination strategy clarifies the action signals of the SP-PFC and hybrid DCCB, which is beneficial for SP-PFC to respond faster to DC faults.

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