Dynamic Improvement of DC Microgrids Using a Dual Approach Based on Virtual Inertia

Mehran Jami, Qobad Shafiee, and Hassan Bevrani

***Abstract*—In this paper, inspired by the concept of virtual inertia in alternating current (AC) systems, a virtual impedance controller is proposed for the dynamic improvement of direct current microgrids (DCMGs). A simple and inexpensive method for injecting inertia into the system is used to adjust the output power of each distributed generation unit without using additional equipment. The proposed controller consists of two components: a virtual capacitor and a virtual inductor. These virtual components can change the rate of change of the DC bus voltage and also improve the transient response. A small-signal analysis is carried out to verify the impact of the proposed control strategy. Numerical simulation studies validate the effectiveness of the proposed solution for increasing the inertia of DCMGs.**

***Index Terms*—DC microgrid, dynamic response, virtual impedance, virtual inertia.**

I. INTRODUCTION

MICROGRIDS (MGs) include distributed generation (DG) units, energy storage systems, and loads that form small generation, transmission, and distribution networks (medium- or low-voltage), which are integrated with power distribution networks [1]. These small-scale power systems are categorized into three types: alternating current (AC), direct current (DC), and hybrid AC-DC MGs. In general, small size, higher efficiency, lower price, higher reliability, and higher power transfer capacity are the most prominent features of DC microgrids (DCMGs) compared with AC microgrids (ACMGs) [2]. Therefore, DCMGs have attracted increasing interest over the past few years.

Owing to the physical characteristics of DG sources, e.g., wind and solar, and the fact that they are usually connected to the network through power electronic converters, their interaction with the network is different from that of traditional networks using bulk steam and water turbines. While the rotating part of a synchronous generator (SG) intrinsically increases the system inertia, this property does not exist in DG sources connected to the network through convertors [3]. Indeed, the inertia slows the natural reaction of the system and provides sufficient time for controllers to function properly. The result of this fact in low-inertia systems is that when a disturbance or imbalance occurs, the reaction time of the system decreases sharply due to the high rate of frequency and voltage changes [4], [5].

The primary control of the power electronic converters is the main factor for low inertia of converter-based systems such as MGs. The primary control of SGs, however, does not affect the swing equation in a short time period due to its slow stimulation and startup. But it affects the power balance equation through the instantaneous available physical source, which is the same energy stored in the rotating volume [6]. For the sources with converter interfaces, this occurs in the opposite way. Similar to the instantaneous physical source in the power converter, the energy is stored in the DC-side capacitor. As a result, power-electronics-interfaced sources can stimulate and start up the primary control, and participate in the power balance equation in a shorter period of time compared with SGs, because they are equipped with a fast DC energy source [7]. Thus, a lack of physical inertia can be compensated potentially by a fast DC-side energy source such as battery, flywheel, or supercapacitor. Another solution to increase the system inertia and control the DC bus voltage in a specified range is to use a DC bus capacitor. Increasing the amount of DC link capacitance leads to an increase in weight, size, and cost. On the other hand, a large DC link capacitor means a large amount of energy stored in the bus. In cases where a short-circuit fault occurs in the bus, the current will generate a severe fault and make the fault isolation quite difficult. This challenge has recently been addressed in the literature. For instance, a modified droop controller is introduced in [8], which minimizes the size of the DC link capacitor, while the bus voltage is still maintained in the allowable range.

The concept of virtual inertia has drawn considerable attention recently to increase the inertia of converter-interfaced systems [9]. In fact, virtual inertia is a subset of a more general concept called a controlled power source (CPS) [1]. Using appropriate voltage and/or frequency and the derivative feedback through an effective control mechanism, the dynamics of the injected power to the system by the CPS can be easily shaped. Unlike ACMGs, the research on virtual inertia for DCMGs is new [10]-[12]. Increasing the inertia of fuel cell generators [13], wind-battery-based grids [14], photovoltaic (PV) systems [15], and virtual inertia control in grid-

---

Manuscript received: May 28, 2020; revised: August 3, 2020; accepted: September 4, 2020. Date of CrossCheck: September 4, 2020. Date of online publication: October 6, 2020.

M. Jami (corresponding author), Q. Shafiee, and H. Bevrani are with the Smart/Micro Grids Research Center (SMGRC), Department of Electrical Engineering, University of Kurdistan, Sanandaj, Iran (e-mail: m.jami@eng.uok.ac.ir; q.shafiee@uok.ac.ir; bevrani@uok.ac.ir).

DOI: 10.35833/MPCE.2020.000343

connected DCMGs has been presented in the literature. However, this is only applicable in the grid-connected operation mode. Furthermore, when distributed energy resources (DERs) such as wind, fuel cell, and solar are not available for power generation, the benefit of inertia emulation through DERs is not available. A virtual DC machine concept is proposed in [16] to mimic the behaviors of DC machines to control a bidirectional DC-DC converter connected with a storage device in a DCMG. In [17], a virtual inertia control is designed to improve the DC bus voltage characteristic of the DCMG in both grid-connected and isolated modes. In [10], [18], a virtual inertia control strategy analogous with virtual synchronous machines is proposed to increase the inertia of the DCMG. However, the integral feedback used in this method does not provide fast inertia in the first moment after disturbances. Furthermore, for the droop-controlled converters in DC grids, the compromise between the damping coefficient and primary voltage regulation needs to be considered. In [19], the size of the DC link capacitor is artificially increased using the virtual capacitor concept. The virtual capacitor control strategy is used to improve the dynamic response of the DC link voltage for the case of reference voltage change, and it does not affect the output current dynamics. However, this strategy does not provide good performance when a load disturbance occurs or the input voltage changes. Reference [20] introduces an inductive impedance loop to efficiently mitigate the low-frequency fluctuations of power and current. A current-voltage droop mechanism using virtual admittance is presented in [21] to improve the system inertia. Although this method results in a quick dynamic response, it does not provide an appropriate function in the steady state. The recent abovementioned research on virtual inertia for DCMG is not useful in the presence of a constant power load (CPL).

The existence of CPLs in DCMGs is the worst-case scenario from the perspective of stability when an instantaneous power imbalance occurs between generation and load [22]. When side-load converters adjust their output voltage to a fixed value, this set, including the converter and its resistance, acts as a CPL from the source-side converter's point of view [23]. The CPLs decrease damping due to the addition of negative resistance to the small-signal model. This causes severe transient fluctuations in the DC bus voltage and finally results in voltage collapse. In [24], the stability of DCMGs, including CPLs, is enhanced by adding passive elements. Although the simple implementation of resistance-capacitance parallel (RC) and resistance-inductance series (RL) filters is interesting, these elements increase the cost and size of MGs [25]. Owing to the nonlinearity of converters and the negative-impedance characteristics of CPLs, nonlinear control strategies have been implemented to stabilize the system [26]. An active damping method based on a supercapacitor energy storage system is presented in [27]. However, the supercapacitor has high cost and remains idle when the DCMG is under steady-state operation. A virtual impedance concept comprising a virtual resistance at the source-side converter [28], a parallel RL branch [29], and a series RL branch [30], is proposed to stabilize the instability between CPLs and their LC input filters. A virtual negative inductor [31] and virtual impedance [30] are constructed using derivative feedback. The constructed virtual negative inductor through the droop control method will counteract the large line inductance, and virtual impedance modifies the output impedance of the source converter to match the input impedance of the cascaded CPL. However, these methods suffer from some disadvantages: ① they are ineffective in providing inertial response; ② when step changes or random fluctuations occur from the intermittent power resources and load power, low-frequency oscillations appear, resulting in lower DC voltage quality.

To address the gaps in the existing literature, a virtual impedance control loop including a virtual capacitor and a virtual inductor is proposed in this paper by using a dual approach based on virtual inertia. The salient features of this paper can be summarized as follows:

1) The proposed virtual impedance control strategy is based on linear configuration feedback. It uses the measurement of the output voltage and inductor current to guarantee the stable operation and to enhance the damping of DCMGs with CPLs. In contrast to the existing virtual-impedance-based stabilizations in [30], [31], which focus only on stability improvement, the proposed controller improves the dynamic response performance with a decreasing rate of change of voltage (RoCoV).

2) Compared with the existing virtual capacitance control methods in [10], [18], and [19], the proposed virtual capacitance control strategy provides a faster inertial response to decrease the RoCoV immediately after disturbances due to the implementation of derivative feedback in the droop control loop. Furthermore, this strategy can handle both resistance loads and CPLs.

3) Small-signal analysis is carried out to study the impact of the virtual components on the system stability. The proposed control strategy is investigated using numerical simulations in the presence of CPL, and its efficiency is verified. In addition, the optimal values of the proposed parameters are obtained.

The rest of this paper is organized as follows. In Section II, the proposed control strategy is introduced based on the virtual impedance concept for DCMGs. Section III describes the small-signal model of DCMGs with CPLs. The stability analysis of the system in the presence of the proposed controller and simulation studies are presented in Section IV. Section V concludes the paper.

II. Virtual Impedance Control Strategy for DCMG

In conventional power systems, the inertia indicates the ability of the system to prevent high-frequency changes by injecting kinetic energy of the rotating part after the occurrence of a fault. Under this condition, the control system of the SG will have enough time to compensate for the active power. In SGs, the swing equation is a relationship that correlates the input mechanical power, output electrical power, and frequency. The imbalance equation, and the kinetic energy stored in the two poles of the SG is given as [3], [10]:

$$P_{set} - P_o = J\omega \frac{\mathrm{d}\omega}{\mathrm{d}t} \approx J\omega_n \frac{\mathrm{d}\omega}{\mathrm{d}t} \tag{1}$$

where P_{set}, P_o, ω, ω_n, and J are the reference active power, output electrical power, angular frequency, nominal angular frequency, and amount of inertia, respectively.

Figure 1 shows a general scheme of these systems [26], [30]. For DCMGs, the amount of inertia is, in fact, the ability of the system to prevent high variation of the DC bus voltage due to turbulence. By imitating (1), the balance current equation in the node connected to the DC link capacitor shown in Fig. 2 is obtained as:

$$\hat{i}_L - \hat{i}_o = C \frac{\mathrm{d}\hat{u}_o}{\mathrm{d}t} \tag{2}$$

where i_L, i_o, u_o, and C are the inductor current, output current, DC bus voltage, and DC bus capacitor, respectively; and the variables with "^" indicate the small-signal deviations. In Fig. 2, u_s is the reference DC voltage.

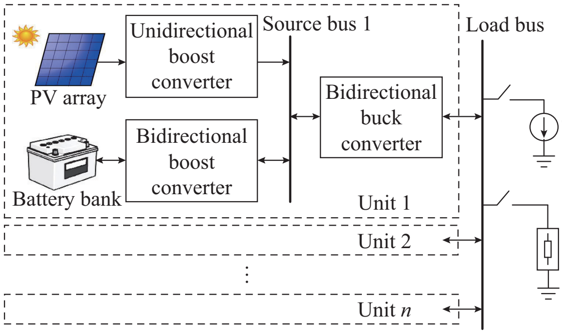


Fig. 1. Structure of a typical DCMG.

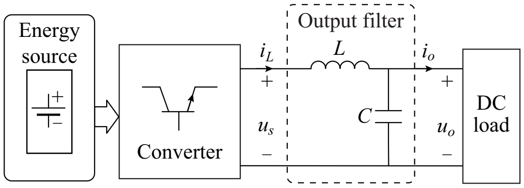


Fig. 2. Typical configuration of a converter-based source supporting a load via capacitance and inductance of output filter.

Comparing (1) with (2), one can note that the DC link capacitor in DCMGs mimics the behavior moment of inertia in AC systems [16], [19]. When turbulence occurs in the output current, the DC link capacitor with rapid active power injection prevents large changes in the DC link voltage. Thus, to increase the inertia in DCMGs, the size of the DC link capacitor must be increased. Obviously, using large capacitors results in a higher price and increases the size and weight of the system, which is not viable for most power-electronics-based applications [14].

Since the virtual impedance control strategy maintains the bus voltage within a certain range, as long as the bus voltage does not exceed the permissible limit during the transient process, it may be a good alternative. Using the concept of virtual impedance for such an application, the amount of current required to be injected can be obtained as:

$$\hat{i}_L^{*} = -C_v \frac{\mathrm{d}\hat{u}_o}{\mathrm{d}t} \tag{3}$$

where i_L^{*} is the amount of current required to be injected; and C_v is the value of the virtual capacitor, respectively. Substituting (3) into (2), we can obtain:

$$\frac{\mathrm{d}\hat{u}_o}{\mathrm{d}t} = -\frac{1}{C + C_v} \hat{i}_o \tag{4}$$

It can be seen from (4) that the virtual capacitance is increased during load changes. As a result, the inertia of the DCMG is improved [21]. Equation (3) models a capacitor parallel to the system capacitor. Taking the Laplace transform of (3), we can obtain:

$$i_L^{*}(s) = I_L - sC_v u_o(s) \tag{5}$$

where I_L is the steady-state value of the inductor current.

The above equation shows that the desired virtual inertial control can be achieved using a droop control framework by adding a capacitive virtual admittance. Multiplying (5) by R_C, the modified virtual impedance droop control function becomes:

$$R_C i_L^{*}(s) = R_C I_L - sR_C C_v u_o(s) \tag{6}$$

Equation (6) can be rewritten as:

$$u_s'^{*}(s) = U_s' - sR_C C_v u_o(s) \tag{7}$$

where $u_s'^{*}(s) = R_C i_L^{*}(s)$ and $U_s' = R_C I_L$.

Similar phenomena can be applied to the voltage balance in the converter output inductance. Taking the idea of (1), the balance voltage equation in the converter output inductor is obtained as:

$$\hat{u}_s - \hat{u}_o = L \frac{\mathrm{d}\hat{i}_L}{\mathrm{d}t} \tag{8}$$

where L is the inductor inductance. The amount of desired injected voltage can be calculated as:

$$\hat{u}_s^{*} = L_v \frac{\mathrm{d}\hat{i}_L}{\mathrm{d}t} \tag{9}$$

where L_v is the value of the virtual inductance. Substituting (9) into (8), we can obtain:

$$\hat{u}_o = -\left(L - L_v\right) \frac{\mathrm{d}\hat{i}_L}{\mathrm{d}t} \tag{10}$$

Equation (9) models a negative inductance series to the system inductor [20], [31]. Using the Laplace transform of (9), the following equation is derived:

$$u_s^{*}(s) = U_s + sL_v i_L(s) \tag{11}$$

To benefit from the properties of both virtual inertia injection and damping strategies, this study proposes a combination of two virtual impedance modules, i.e., a virtual capacitor and a virtual negative inductor, in addition to the conventional virtual resistance (droop mechanism), as shown in Fig. 3, where R_d is the conventional virtual resistance in droop control.

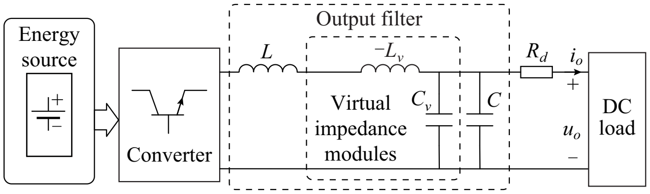


Fig. 3. Proposed virtual impedance strategy.

III. SMALL-SIGNAL MODELING OF DCMG WITH CPLs

A. Configuration of DCMG

A typical structure of a DCMG is shown in Fig. 1. Without loss of generality, one unit with two types of renewable energy sources (RESs), a PV array and a battery bank, are considered. The DCMG shown in Fig. 1 employs a three-level configuration. At the first level, namely the source stage, an interface converter is employed for the PV array to absorb the maximum available power. The converter interfaced to the battery bank is used to generate a constant output voltage. The second level utilizes a bidirectional converter to establish the local output bus. The third level is the common load bus where the CPLs are connected. Different voltage levels can be used in DCMGs. Here, the rated output voltages of the PV and battery are 110 V and 114 V, respectively. The output voltage, i.e., the source bus voltage, is controlled as 380 V. Further, the output voltage of the second stage is selected as 200 V, i.e., the rated voltage of the local output bus is 200 V. Due to the nominal voltage of each bus, different types of interface converters are selected. For PVs at the first stage, a unidirectional boost converter is used, while a bidirectional boost converter is selected for the battery to achieve both the charging and discharging operations. For the interface converter at the second stage, a bidirectional buck converter is selected. For a CPL connected at the common load bus, a unidirectional buck converter is selected.

B. Control Objectives

Based on the concept of virtual inertia, a virtual impedance control approach is developed to provide the following properties.

1) Stability enhancement: one of the control objectives is to tackle the CPL instability by introducing a virtual impedance control. Specifically, the poles of the small-signal model should all be located in the left half of the s-plane.

2) Effective tradeoff between RoCoV and settling time: the virtual capacitance is constrained to limit the RoCoV in a certain range, i.e., $RoCoV<RoCoV_{\max}$. However, by increasing C_v, the settling time increases, and the dynamic response slowly increases. Therefore, an effective tradeoff between RoCoV and the settling time is required.

3) Damping improvement: the virtual inductance is constrained to increase the damping. As a result, the voltage deviation decreases. The proper values of the parameters are selected in Section IV-B by tracing the system eigenvalues.

C. Small-signal Model of DCMG with CPLs

The dominant dynamics in the conventional power system include SGs and their corresponding control loops. In the systems with low inertia, however, it is necessary to use the precise model of power electronic converters, their control methods, and the constraints. In order to study the effectiveness of the proposed virtual impedance function, a precise and comprehensive model of DCMGs needs to be considered. Different types of interface converters are utilized at each stage. A detailed analysis of the overall system model is discussed as follows. Here, the indexes 1-4 are used for the PV unidirectional boost converter, the battery bidirectional boost converter, the bidirectional buck converter between the local source bus and the local output bus, and the CPL unidirectional buck converter, respectively. For the unidirectional boost converters used for PVs, the converter topology is shown in Fig. 4(a). In order to derive the detailed model of the converter, state-space averaging is employed [26], [30], [32].

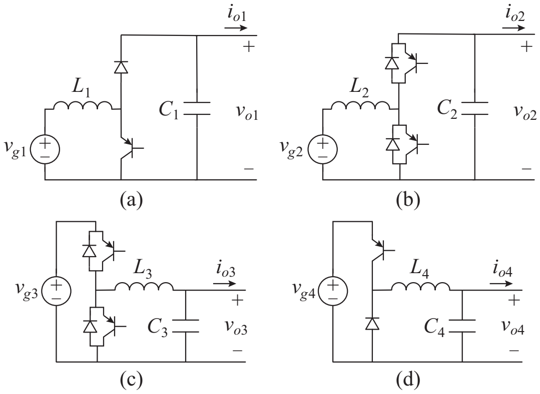


Fig. 4. Topologies of interface converters with different levels. (a) Unidirectional boost converter. (b) Bidirectional boost converter. (c) Bidirectional buck converter. (d) Unidirectional buck converter.

When the switch is turned on or off, the circuit topology changes accordingly. If the switch turns on, it yields:

$$\begin{cases} L_1\dfrac{\mathrm{d}i_{L1}}{\mathrm{d}t}=v_{g1} \\ C_1\dfrac{\mathrm{d}v_{C1}}{\mathrm{d}t}=-i_{o1} \end{cases} \tag{12}$$

where L_1, C_1, i_{L1}, v_{C1}, v_{g1}, and i_{o1} are the inductance, capacitance, inductor current, capacitor voltage, input voltage, and output current, respectively. If the switch is turned off, it yields:

$$\begin{cases} L_1\dfrac{\mathrm{d}i_{L1}}{\mathrm{d}t}=v_{g1}-v_{C1} \\ C_1\dfrac{\mathrm{d}v_{C1}}{\mathrm{d}t}=i_{L1}-i_{o1} \end{cases} \tag{13}$$

By using state-space averaging, the state-space equation can be derived as:

$$\begin{cases} L_1\dfrac{\mathrm{d}i_{L1}}{\mathrm{d}t}=v_{g1}-\left(1-d_1\right)v_{C1} \\ C_1\dfrac{\mathrm{d}v_{C1}}{\mathrm{d}t}=\left(1-d_1\right)i_{L1}-i_{o1} \end{cases} \tag{14}$$

where d_1 is the duty cycle for the on-state of the switch. Based on the results in (14), the small-signal model is achieved as:

$$\begin{cases} L_1\dfrac{\mathrm{d}\hat{i}_{L1}}{\mathrm{d}t}=\hat{v}_{g1}-\left(1-D_1\right)\hat{v}_{C1}+V_{C1}\hat{d}_1 \\ C_1\dfrac{\mathrm{d}\hat{v}_{C1}}{\mathrm{d}t}=\left(1-D_1\right)\hat{i}_{L1}-I_{L1}\hat{d}_1-\hat{i}_{o1} \end{cases} \tag{15}$$

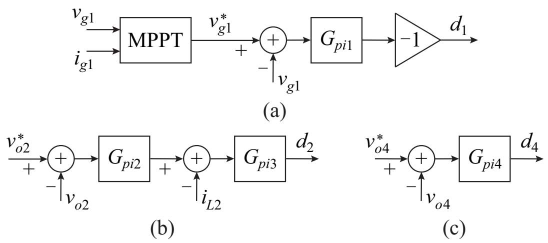
where V_{C1}, I_{L1}, and D_1 are the steady-state values. By transforming the linear small-signal model in (15) into the frequency domain and combining the results, we can obtain:

$$\hat{v}_{C1}(s)=G_{vg1}\hat{v}_{g1}(s)+G_{vd1}\hat{d}_1(s)-z_{o1}\hat{i}_{o1}(s) \tag{16}$$

$$\begin{cases} G_{vg1} = \dfrac{1-D_1}{L_1 C_1 s^2 + \left(1-D_1\right)^2} \\ G_{vd1} = \dfrac{\left(1-D_1\right)V_{C1} - I_{L1} L_1 s}{L_1 C_1 s^2 + \left(1-D_1\right)^2} \\ z_{o1} = \dfrac{L_1 s}{L_1 C_1 s^2 + \left(1-D_1\right)^2} \end{cases} \tag{17}$$

Since the interface converter for PV is used to realize maximum power point tracking (MPPT) without the need to establish the voltage of the source bus, a basic control diagram shown in Fig. 5(a) is used, where G_{pi1}-G_{pi4} are conventional proportional-integral (PI) controllers. The PI controller is composed of proportional gain K_p and integral gain K_i. Its transfer function is expressed as $G_{pij} = K_{pj} + K_{ij}/s$. Hence, the small-signal model of the control diagram in the frequency domain is achieved as:

$$\hat{d}_1(s) = -\left(\hat{v}_{g1}^*(s) - \hat{v}_{g1}(s)\right) G_{pi1} \tag{18}$$



(a)

(b)

(c)

Fig. 5. Control diagram of different interface converters. (a) Unidirectional boost converter. (b) Bidirectional boost converter. (c) Unidirectional buck converter.

Analyzing the simultaneous equations (16) and (18), we can obtain:

$$\hat{v}_{C1}(s) = G_{11}\hat{v}_{g1}(s) + G_{12}\hat{v}_{g1}^*(s) - Z_{o1}\hat{i}_{o1}(s) \tag{19}$$

$$\begin{cases} G_{11} = G_{vg1} + G_{vd1} G_{pi1} \\ G_{12} = -G_{vd1} G_{pi1} \\ Z_{o1} = z_{o1} \end{cases} \tag{20}$$

The above discussion is for the modeling of a unidirectional boost converter used for PV. For the bidirectional boost converter used for the battery, the analysis is the same as that for the PV converter. The basic topology of the bidirectional boost converter is shown in Fig. 4(b). To avoid repetition, no detailed procedures are shown below, but the final equation is given as:

$$\hat{v}_{C2}(s) = G_{vg2}\hat{v}_{g2}(s) + G_{vd2}\hat{d}_2(s) - z_{o2}\hat{i}_{o2}(s) \tag{21}$$

The battery converter is used to establish the source bus. Thus, its basic control diagram is shown in Fig. 5(b). Based on this control diagram, the small-signal model is achieved:

$$\hat{d}_2(s) = \hat{v}_{g2}^*(s) G_{pi2} G_{pi3} - \hat{v}_{C2}(s) G_{pi2} G_{pi3} - \hat{i}_{L2}(s) G_{pi3} \tag{22}$$

By solving the simultaneous equations of (21) and (22), we can obtain:

$$\hat{v}_{C2}(s) = G_{21}\hat{v}_{g2}(s) + G_{22}\hat{v}_{o2}^*(s) - Z_{o2}\hat{i}_{o2}(s) \tag{23}$$

$$\begin{cases} G_{21} = \dfrac{1}{T_2}\left[\left(1-D_2\right) + I_{L2} G_{pi3}\right] \\ G_{22} = \dfrac{1}{T_2}\Big\{V_{C2} G_{pi2} G_{pi3}\left[\left(1-D_2\right) + I_{L2} G_{pi3}\right] - \\ \qquad \left(I_{L2} G_{pi2} G_{pi3}\right)\left(L_2 s + V_{C2} G_{pi3}\right)\Big\} \\ Z_{o2} = \dfrac{1}{T_2}\left(L_2 s + V_{C2} G_{pi3}\right) \\ T_2 = \left(C_2 s - I_{L2} G_{pi2} G_{pi3}\right)\left(L_2 s + V_{C2} G_{pi3}\right) + \\ \qquad \left[\left(1-D_2\right) + I_{L2} G_{pi3}\right]\left[\left(1-D_2\right) + V_{C2} G_{pi2} G_{pi3}\right] \end{cases} \tag{24}$$

For the point-of-load (POL) converter, a unidirectional buck converter with a resistor is selected as an example to represent the CPL, as shown in Fig. 4(d). Power converters such as buck converters are used due to their tight output voltage control capability, which enables them to respond almost immediately to system changes [23]. A conventional PI controller G_{pi4} is used to regulate the output voltage of the POL converter, as shown in Fig. 5(c). In this case, the small-signal dynamics can be represented by the closed-loop input impedance of the POL converter [23], [30]:

$$Z_L = \frac{R_L C_4 L_4 s^3 + L_4 s^2 + R_L\left(1 + V_{g4} k_{p4}\right)s + R_L V_{g4} k_{i4}}{R_L C_4 D_4^2 s^2 + \left(D_4^2 - k_{p4} D_4^2 V_{g4}\right)s - k_{i4} D_4^2 V_{g4}} \tag{25}$$

where Z_L and R_L are the closed-loop input impedance and load resistance of the POL converter, respectively; C_4 and L_4 are the capacitance and inductance of the output filter, respectively; V_{g4} is the steady-state input voltage of the POL converter; k_{p4} and k_{i4} are the proportional and integral terms of the PI controller, respectively; and D_4 is the duty cycle in the steady state. Equation (25) is more accurate than the traditional approximation by using a pure negative resistance equal to $Z_L = -R_L/D_4^2$ [27], [29]. The load connected to the common load bus is a constant impedance load, and $Z_L = R_L$.

For the bidirectional buck converter between the local source bus (380 V) and local output bus (200 V), the basic topology is shown in Fig. 4(c). By using a similar procedure to that used above and assuming that the deviation of input voltage in the source stage is zero, it can be concluded that:

$$\begin{cases} L_3 \dfrac{\mathrm{d}\hat{i}_{L3}}{\mathrm{d}t} = D_3 \hat{v}_{g3} - \hat{v}_{C3} + V_{g3}\hat{d}_3 \\ C_3 \dfrac{\mathrm{d}\hat{v}_{C3}}{\mathrm{d}t} = \hat{i}_{L3} - \hat{i}_{o3} \\ \hat{i}_{g3} = D_3 \hat{i}_{L3} + I_{L3}\hat{d}_3 \\ \hat{i}_{o3} = \dfrac{\hat{v}_{C3}}{Z_L} \\ \hat{i}_{g3} = -\dfrac{\hat{v}_{g3}}{Z_o} \end{cases} \tag{26}$$

$$Z_o = \frac{Z_{o1} Z_{o2}}{Z_{o1} + Z_{o2}} \tag{27}$$

The general scheme of the proposed virtual impedance loop implemented in the primary control level is illustrated in Fig. 6. Without the loss of generality, a DC-DC buck converter is utilized. The control mechanism applied to the system consists of three modules: inner loop (voltage and current controllers), a virtual impedance loop, and *V-I* droop loop. The voltage and current controllers employ conventional PI controllers, as they have zero steady-state error with simple structure and easy adjustment. The droop mechanism acts as a proportional gain used for power sharing in the presence of multiple DG sources. The pure differentiator may bring undesired high-frequency noise to the system. This can be solved by constructing a first-order low-pass filter (LPF) in series with derivative feedback [12]. Considering the control diagram in Fig. 6, we can obtain:

$$\begin{aligned}\hat{d}_3(s) &= \hat{v}_{C3}^*(s)G_{pi5}G_{pi6} - \hat{i}_{o3}(s)R_dG_{pi5}G_{pi6} - \hat{i}_{L3}(s)G_{pi6}\cdot \\ &\quad \left(1 - sL_vG_{pi5}G_{LPF2}\right) - \hat{v}_{C3}(s)G_{pi5}G_{pi6}\left(1 + sR_CC_vG_{LPF1}\right)\end{aligned} \tag{28}$$

where $G_{LPF1} = 1/\left(\tau_C s + 1\right)$, τ_C is the time constant of LPF1; and $G_{LPF2} = 1/\left(\tau_L s + 1\right)$, τ_L is the time constant of LPF2. Considering (26), (27), and (28), we can obtain:

$$\hat{v}_{C3}(s) = G_{31}\hat{v}_{C3}^*(s) \tag{29}$$

where G_{31} is given by:

$$G_{31} = \frac{G_{pi5}G_{pi6}\left(V_{g3} - D_3Z_oI_{L3}\right)}{1 + \left(C_3s + \dfrac{1}{Z_L}\right)\left[L_3s + D_3^2Z_o + G_{pi6}\left(V_{g3} - D_3Z_oI_{L3}\right)\left(1 - sL_vG_{pi5}G_{LPF2}\right)\right] + G_{pi5}G_{pi6}\left(V_{g3} - D_3Z_oI_{L3}\right)\left(1 + \dfrac{R_d}{Z_L} + sR_CC_vG_{LPF1}\right)} \tag{30}$$

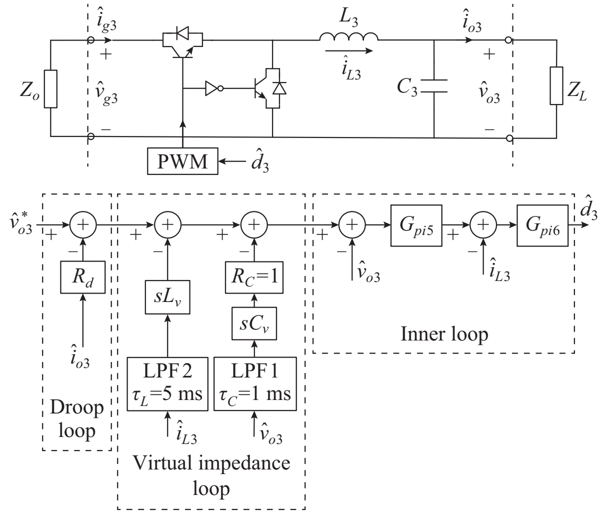


Fig. 6. Proposed control strategy for bidirectional buck converters.

IV. SIMULATION RESULTS

To validate the effectiveness of the proposed control strategy for DCMGs, the test system shown in Fig. 1 is simulated in MATLAB/Simulink environment. The values of the parameters are listed in Tables I and II.

A. Stability Analysis of Closed-loop System

This sub-section focuses on analyzing the stability and improving the damping of an interfaced bidirectional buck converter in a DCMG equipped with the proposed control loop. By analyzing the eigenvalues, the relationship between system stability and various control parameters, including the virtual capacitor and virtual inductor, is reviewed.

In order to obtain a stable system, the dominant poles of the small-signal model in (30) should all be located in the left half of the *s*-plane. The effectiveness of the proposed controller with CPLs can also be tested by changing the values of the virtual impedances, as shown in Fig. 7. The trajectory of the dominant poles is shown in Fig. 7(a) with changing virtual capacitance $0 < C_v < 0.03$ F, $L_v = 0.001$ H, and $P_o = 4$ kW. Once the value of C_v increases, the dominant pole is a pure real number and moves toward the imaginary axis.

TABLE I
SYSTEM PARAMETERS OF DCMG

System	Parameter	Value
PV system	Input inductor L_1	6 mH
	Output capacitor C_1	0.5 mF
	Rated input voltage V_{g1}	110 V
	Rated output voltage V_{o1}	300 V
Battery system	Input inductor L_2	2.5 mH
	Output capacitor C_2	0.8 mF
	Rated input voltage V_{g2}	114 V
	Rated output voltage V_{o2}	380 V
Interface converter	Output inductor L_3	5 mH
	Output capacitor C_3	1.2 mF
	Rated input voltage V_{g3}	380 V
	Rated output voltage V_{o3}	200 V
Load	Output inductor L_4	0.5 mH
	Output capacitor C_4	0.1 mF
	Load power	4 kW
	Rated output voltage V_{o4}	100 V

By increasing C_v, the damping ratio of the dominant poles increases and the response speed decreases. The trajectory of the dominant poles is shown in Fig. 7(b) with changing virtual inductance $0 < L_v < 0.013$ H, $C_v = 0.001$ F, and $P_o = 4$ kW. By increasing L_v, the damping ratio of the dominant poles increases and the system behaves like a second-order system. The unstable system trajectory when gradually increasing the load power is shown in Fig. 7(c) with $C_v = 0.001$ F and $L_v = 0.001$ H. It can be seen that the dominant poles move toward the unstable region. Increasing the power load deteriorates the damping and causes instability.

Figure 8 shows the dominant low-frequency modes of the system when the time constant of the LPFs increases. By selecting proper time constants, i.e., $\tau_C > 0$ and $\tau_L > 0.5$ ms, the unstable poles move to the stable region. Hence, the system stability is ensured. By increasing τ, the damping factor of the system is improved. Therefore, the inflection point of the system root-locus is the optimal one for time constants $\tau_C = 1$ ms and $\tau_L = 5$ ms.

TABLE II
CONTROLLER PARAMETERS OF DCMG

System	Parameter	Value
PV system	K_{p1}	0.001
	K_{i1}	1
Battery system	K_{p2}	0.1
	K_{p3}	0.4
	K_{i2}	20
	K_{i3}	25
Interface converter	K_{p5}	0.4
	K_{p6}	0.1
	R_d	0.25
	K_{i5}	50
	K_{i6}	100
	f_{sw}	20 kHz
Load	K_{p4}	0.1
	K_{i4}	100

B. Parameter Selection

The following steps summarize the proposed control strategy for parameter selection.

1) In order to avoid the interference between the two cascaded loops in the interfaced buck converter, the bandwidth of the outer voltage control loop is selected to be one-tenth of the inner current control loop bandwidth. Therefore, the bandwidth of the inner current loop can be designed faster in the range of kilohertz, and the transfer function (30) can be simplified as:

$$G_{31} = \frac{G_{pi5}}{\left(C_3 s + 1/Z_L\right)\left(1 - sL_v G_{pi5} G_{LPF2}\right) + G_{pi5}\left(1 + R_d/Z_L + sR_C C_v G_{LPF1}\right)} \tag{31}$$

2) The parameter R_d is tuned using the method given in [31], [33] as:

$$R_d = \frac{v_{o3,\min} \Delta v_{o3}}{P_{\max}} \tag{32}$$

where Δv_{o3} is the maximum allowed deviation of the MG voltage; $P_{\max}$ is the maximum output power from the converter; and $v_{o3,\min}$ is the minimum allowed MG voltage.

3) In order to obtain a stable system, the coefficients of the characteristic equation in (31) should be positive. So we can obtain:

$$L_v < \frac{\tau_L}{K_{p5}} \tag{33}$$

As a result, the first control objective can be achieved.

4) From (31), the parameter C_v is selected using RoCoV:

$$\left| RoCoV \right| = \left. \frac{\left| \Delta v_{o3} \right|}{\Delta t} \right|_{\Delta t \to 0} \approx \frac{\left| \Delta v_{o3}^{*} \right| K_{p5}}{C_3 + C_v K_{p5}} \tag{34}$$

It is assumed that the value of $RoCoV$ does not exceed $RoCoV_{\max}$. So we can obtain:

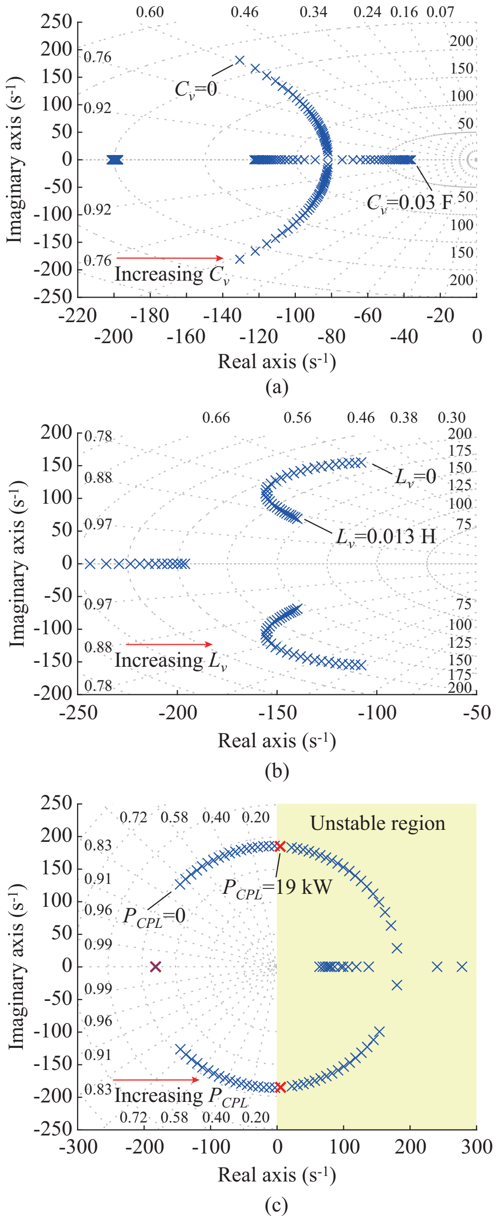


Fig. 7. Trace of system eigenvalues. (a) Varying C_v for $L_v = 1$ mH and $CPL = 4$ kW. (b) Varying L_v for $C_v = 0.001$ F and $CPL = 4$ kW. (c) Varying P_{CPL} for $L_v = 1$ mH and $C_v = 0.001$ F.

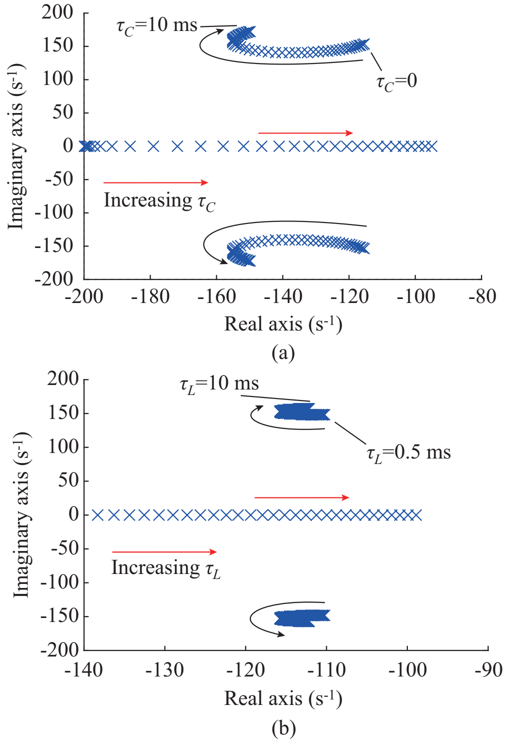
$$C_v \geq \frac{\left| \Delta v_{o3}^{*} \right|}{RoCoV_{\max}} - \frac{C_3}{K_{p5}} \tag{35}$$

As a result, the second control objective can thus be achieved.

5) The parameters τ_L and τ_C are tuned by using the trace of system eigenvalues in Fig. 8. In order to achieve the maximum damping, the inflection point of the system root-locus will be the optimal one for the time constants, and $L_v = L_{v,\max} = \tau_L / K_{p5}$. The third control objective can thus be achieved.

C. Case I: Evaluating DCMG Test System Augmented with Proposed Virtual Inertia

A typical DCMG, including a PV, a battery, and a CPL, is used to verify the proposed control strategy.



(a)

(b)

Fig. 8. Trace of system eigenvalues. (a) Varying τ_C for $L_v = 1$ mH, $C_v = 1$ mF, and $CPL = 4$ kW. (b) Varying τ_L for $L_v = 1$ mH, $C_v = 1$ mF, and $CPL = 4$ kW.

For the PV, as mentioned above, a unidirectional boost converter is used. It works in the MPPT mode to track the maximum power from the solar panel. The bidirectional boost converter for the battery is used to establish the local source bus with voltage and current control loops. The source bus voltage is regulated at 380 V by changing the injected solar power. By using the bidirectional buck converter for the interface converter, the load bus of the DG unit is established. The load bus is regulated at a rated value of 200 V. The existence of the CPLs in DCMGs is the worst-case scenario from the perspective of stability. Thus, we assume that the CPL power rate is 4 kW. The PV output power, battery output power, and CPL power are shown in Fig. 9 when the PV output power reference changes. The PV output power follows its reference value and with the battery feed load power. When the PV output power is greater than the load power, the difference in their power is stored in the battery (0.4 s$<t<0.5$ s).

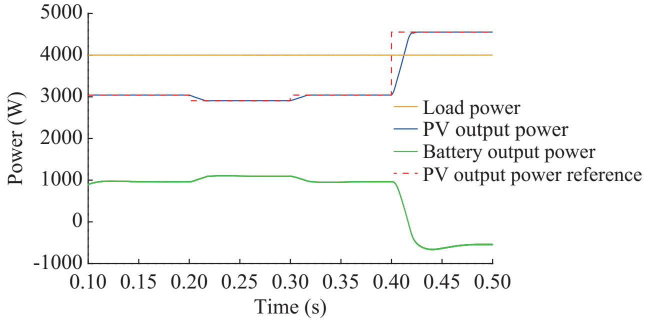


Fig. 9. Output power of DCMG units with changing PV power reference when equipped with proposed virtual inertia control loop.

The PV output voltage, the source bus voltage, and the load bus voltage are shown in Fig. 10 when the PV output power reference changes. It should be noted that the output voltage of the load bus is slightly lower than its rated value because of the usage of the droop mechanism in the control system.

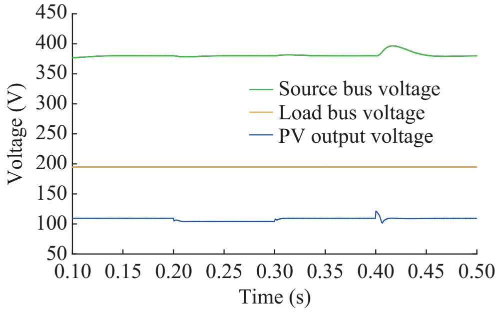
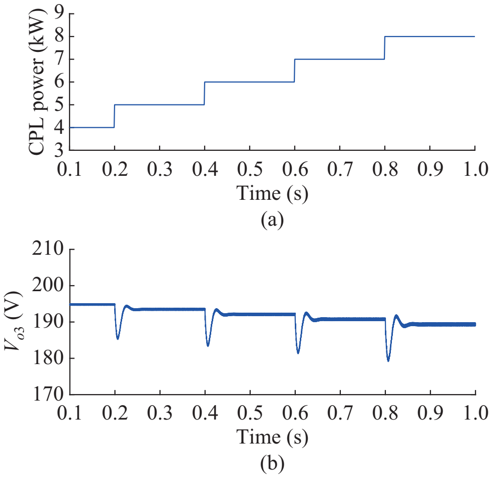


Fig. 10. Output voltage of DCMG units with changing PV power reference when equipped with proposed virtual inertia control loop.

D. Case II: Performance of Proposed Solution Under Reference Voltage and Load Power

A continuous load step-up change occurs at the load bus. In particular, the CPL changes following the sequences of 4, 5, 6, 7, and 8 kW. By using the proposed virtual inertia and droop control, as shown in Fig. 11(b), the stable operation is guaranteed. Furthermore, the performance of the system with a continuous voltage reference step-up change is also tested. In particular, the rated voltage of the load bus is set to be the sequence of 200, 220, 240, 260, and 280 V. It can be seen in Fig. 12 that with the proposed virtual inertia, the stable operation is maintained throughout the entire process.



(a)

(b)

Fig. 11. System performance under changes of operating point. (a) Load power step-up. (b) DC output voltage.

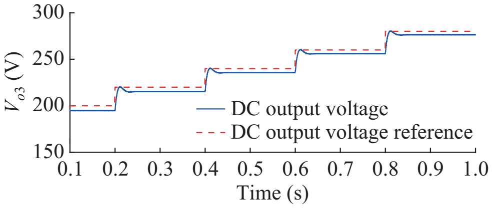
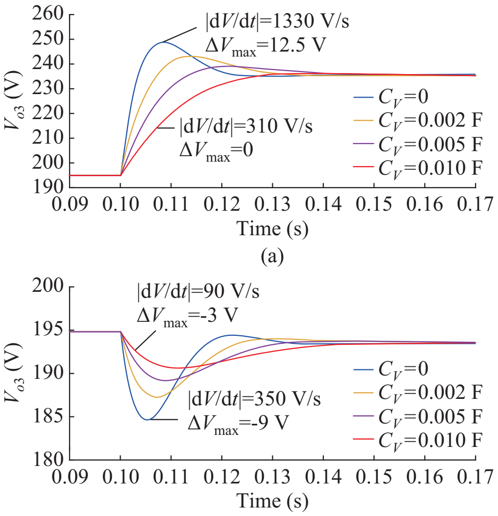


Fig. 12. System performance under voltage reference step-up.

E. Case III: Impact of Virtual Impedance

Figure 13 shows the dynamic response of the DC bus voltage when the value of the virtual capacitor changes and other system parameters are constant. In Fig. 13(a), the reference voltage is increased by 0.2 p. u. from V_{ref}=200 V to V_{ref}=240 V at t=0.1 s. When C_v increases, the dynamic response of the DC bus output voltage slows down and prevents sudden voltage changes due to turbulence. Therefore, the RoCoV decreases and the inertia increases. The RoCoV without the virtual capacitance is approximately 1330 V/s. By contrast, when the proposed virtual capacitance loop (for C_v=0.01 F) is considered, the RoCoV can be limited to 310 V/s. Therefore, a 76% RoCoV reduction is achieved using the proposed virtual capacitance loop. Furthermore, the maximum voltage deviation can be reduced from 12.5 V to 0, indicating a 100% improvement. In Fig. 13(b), the DC bus output voltage is shown when the load power is increased by 0.25 p.u. from the initial value of P_o=4 kW, to the final value of P_o=5 kW at t=0.1 s. As C_v increases, the dynamic response of the DC bus output voltage slows down and the RoCoV decreases. One can observe that the virtual capacitor C_v can reduce the fluctuations of the DC bus output voltage while improving the dynamic response of the system. Therefore, with the proposed virtual capacitance (for C_v=0.01 F), the RoCoV and the maximum voltage deviation are reduced by 74% and 66%, respectively.

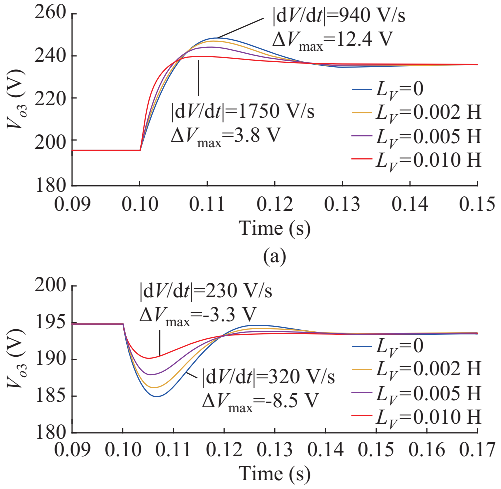


(a)

(b)

Fig. 13. Impact of virtual capacitance for DCMG for L_v=0.001 H, R_d= 0.25 Ω, and *CPL*=4 kW. (a) Load bus reference voltage increases by 0.2 p.u. at t=0.1 s. (b) Load power increases by 0.25 p.u. at t=0.1 s.

Figure 14 shows the dynamic response of the DC bus voltage when the value of the virtual inductance changes and other system parameters are constant. In Fig. 14(a), the reference voltage increases by 0.2 p.u. from V_{ref}=200 V to V_{ref}= 240 V at t=0.1 s. When L_v increases, the DC bus output voltage performance is improved because of the significant reduction of the overshoot and oscillations. Hence, with the proposed virtual inductance (for L_v=0.01 H), the maximum voltage deviation is reduced by 69%. However, the RoCoV increases. In Fig. 14(b), the DC bus output voltage is shown when the load power increases by 0.25 p.u. from the initial value of P_o=4 kW to the final value of P_o=5 kW at t=0.1 s. As L_v increases, the maximum voltage deviation can be reduced. From Fig. 14(b), it can be seen that the RoCoV and the maximum voltage deviation are reduced by 28% and 61%, respectively.

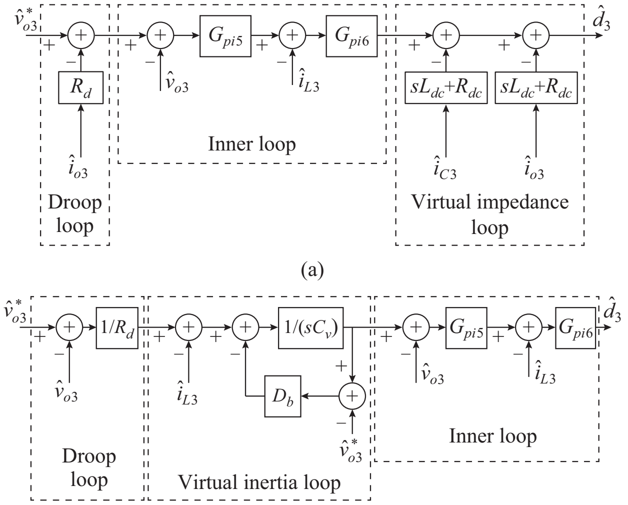


(a)

(b)

Fig. 14. Impact of virtual inductance for DCMG for C_v=0.001 F, R_d=0.25 Ω, and *CPL*=4 kW. (a) Load bus reference voltage increases by 0.2 p.u. at t=0.1 s. (b) Load power increases by 0.25 p.u. at t=0.1 s.

The results obtained using the proposed control strategy are compared with those obtained using other techniques in order to identify the advantages of the proposed technique. Figure 15 shows the control structure of the virtual impedance method [30] and the virtual capacitor method [10], [18], [19].



(a)

(b)

Fig. 15. Two different control structures. (a) Virtual impedance method. (b) Virtual capacitor method.

Figure 16 shows the comparison of simulation results between these methods and the proposed control strategy with the same system parameters, loading conditions, and a 25% step change of load power at t=0.2 s. In order to obtain a better comparison, the same RoCoV and steady-state values are considered in all three methods. The mentioned methods are compared using key indicators of the performance of the algorithm, i.e., the RoCoV after load change, the maximum voltage deviations from the steady-state value $v_{o3,ss}$, and the settling time. A comparison of the main parameters is shown in Table III, where the indicators are: $|RoCoV|\big|_{\Delta t=0.0005\text{ s}}=\dfrac{|\Delta v_{o3}|}{\Delta t}=\dfrac{|v_{o3}(t=0.00005\text{ s})-v_{o3}(t=0)|}{0.0005}$; $|\Delta v_{o3,\max}|=|v_{o3,\min}-v_{o3,ss}|$, which is the maximum voltage deviation from the steady-state value; and $v_{o3\text{-}pu}=(v_{o3}-v_{o3,ss})/v_{o3,ss}$. It can be observed that the proposed control strategy provides a better transient response, shorter settling time, smaller undershoot, and no overshoot in comparison with other control techniques. Therefore, the proposed control strategy achieves the control objectives.

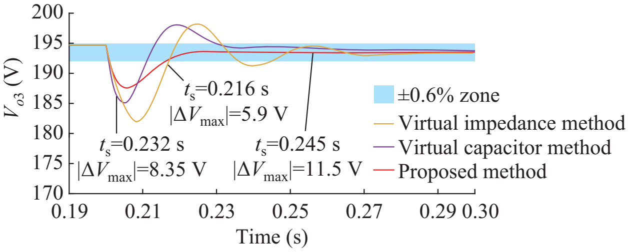


Fig. 16. Comparison between virtual impedance, virtual capacitor, and proposed methods.

TABLE III
COMPARISON OF PROPOSED METHOD WITH EXISTING METHODS

Method	Control parameters	Indicator		
		$\lvert RoCoV\rvert\big\rvert_{\Delta t=0.0005\text{ s}}$ (V/s)	$\lvert\Delta V_{o3,\max}\rvert$ (V)	t_s ($v_{o3\text{-}pu}$<0.6 %) (s)
Virtual capacitor [10], [18], [19]	$D_b=0.1$ S, $C_v=0.1$ F	4400	8.35	0.232
Virtual impedance [30]	$L_{DC}=0.3$ H, $R_{DC}=0.01$ Ω, $L'_{DC}=0.1$ H, $R'_{DC}=0.01$ Ω	4400	11.50	0.245
Proposed	$L_v=0.005$ H, $C_v=0.001$ F, $\tau_L=5$ ms, $\tau_C=1$ ms	4400	5.90	0.216

V. CONCLUSION

Inspired by the concept of virtual inertia in AC systems, this paper introduced a virtual impedance control loop for the dynamic improvement of DCMGs. The proposed control strategy includes two modules: a virtual capacitor and a virtual negative inductor. The results, run with the proposed virtual impedances for voltage reference and load power changes, show a stable operation in the presence of CPLs. The proposed control strategy offers multiple advantages compared with the existing control techniques: ① the virtual capacitor can properly reduce the rate of DC bus voltage changes independent of loading conditions (CPL and/or resistive load) with no overshoot; ② the virtual inductance enhances the damping of DCMG with CPLs and reduces the maximum voltage deviation; ③ the speed of the response is increased by decreasing the settling time. The provided model and small-signal stability studies are used to design the best virtual parameters. Stability analysis and numerical simulations show that the virtual capacitor and inductor provide better performance when the reference voltage and load current change.

REFERENCES

[1] H. Bevrani, B. Francois, and T. Ise, *Microgrid Dynamics and Control*. New York: Wiley, 2017.

[2] T. Dragičević, X. Lu, J. C. Vasquez *et al*., "DC microgrids–Part I: a review of control strategies and stabilization techniques," *IEEE Transactions on Power Electronics*, vol. 31, no. 7, pp. 4876-4891, Jul. 2016.

[3] H. Bevrani, T. Ise, and Y. Miura, "Virtual synchronous generators: a survey and new perspectives," *International Journal of Electrical Power & Energy Systems*, vol. 54, pp. 244-254, Jan. 2014.

[4] J. Fang, H. Li, Y. Tang *et al*., "Distributed power system virtual inertia implemented by grid-connected power converters," *IEEE Transactions on Power Electronics*, vol. 33, no. 10, pp. 8488-8499, Oct. 2018.

[5] J. Liu, Y. Miura, H. Bevrani *et al*., "Enhanced virtual synchronous generator control for parallel inverters in microgrids," *IEEE Transactions on Smart Grid*, vol. 8, no. 5, pp. 2268-2277, Sept. 2017.

[6] U. Tamrakar, D. Shrestha, M. Maharjan *et al*., "Virtual inertia: current trends and future directions," *Applied Sciences*, vol. 7, no. 7, pp. 1-29, Jun. 2017.

[7] F. Milano, F. Dörfler, G. Hug *et al*., "Foundations and challenges of low-inertia systems," in *Proceedings of 2018 IEEE Power Systems Computation Conference (PSCC)*, Dublin, Ireland, Jun. 2018, pp. 1-25.

[8] L. Guangyuan, P. Mattavelli, and S. Saggini, "Design of droop controllers for converters in DC microgrids towards reducing bus," in *Proceedings of 2018 20th European Conference on Power Electronics and Applications (EPE' 18 ECCE Europe)*, Riga, Latvia, Nov. 2018, pp. 1-10.

[9] J. Fang, H. Li, Y. Tang *et al*., "Distributed power system virtual inertia implemented by grid-connected power converters," *IEEE Transactions on Power Electronics*, vol. 33, no. 10, pp. 8488-8499, Oct. 2018.

[10] W. Wu, Y. Chen, A. Luo *et al*., "A virtual inertia control strategy for DC microgrids analogized with virtual synchronous machines," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 7, pp. 6005-6016, Jul. 2017.

[11] Y. Li, L. He, F. Liu *et al*., "Flexible voltage control strategy considering distributed energy storages for DC distribution network," *IEEE Transactions on Smart Grid*, vol. 10, no. 1, pp. 163-172, Jan. 2019.

[12] E. Rakhshani and P. Rodriguez, "Inertia emulation in AC/DC interconnected power systems using derivative technique considering frequency measurement effects," *IEEE Transactions on Power Systems*, vol. 32, no. 5, pp. 3338-3351, Sept. 2017.

[13] Y. Han, Y. Pu, Q. Li *et al*., "Coordinated power control with virtual inertia for full cell-based DC microgrids cluster," *International Journal of Hydrogen Energy*, vol. 44, no. 46, pp. 25207-25220, Sept. 2019.

[14] X. Zhu, Z. Xie, S. Jing *et al*., "Distributed virtual inertia control and stability analysis of DC microgrid," *IET Generation, Transmission & Distribution*, vol. 12, no. 14, pp. 3477-3486, May 2018.

[15] W. Im, C. Wang, W. Liu *et al*., "Distributed virtual inertia based control of mutiple photovoltaic systems in autonomous microgrid," *IEEE/CAA Journal of Automatica Sinica*, vol. 4, no. 3, pp. 512-519, Jul. 2017.

[16] S. Samanta, J. P. Mishra, and B. K. Roy, "Virtual DC machine: an inertia emulation and control technique for a bidirectional DC-DC converter in a DC microgrid," *IET Electric Power Applications*, vol. 12, no. 6, pp. 847-884, Mar. 2018.

[17] S. Samanta, J. P. Mishra, and B. K. Roy, "Implementation of a virtual inertia control for inertia enhancement of a DC microgrid under both grid connected and isolated operation," *Computers & Electrical Engineering*, vol. 76, pp. 283-298, Jun. 2019.

[18] E. Unamuno and J. A. Barrena, "Equivalence of primary control strategies for AC and DC microgrids," *Energies*, vol. 10, no. 1, pp. 1-13, Jan. 2017.

[19] E. Unamuno and J. A. Barrena, "Design and small-signal stability analysis of a virtual-capacitor control for DC microgrids," in *Proceedings of 2017 19th European Conference on Power Electronics and Applications (EPE' 17 ECCE Europe)*, Warsaw, Poland, Sept. 2017, pp. 1-10.

[20] M. Hamzeh, M. Ghafouri, H. Karimi *et al*., "Power oscillations damping in DC microgrids," *IEEE Transactions on Energy Conversion*, vol. 31, no. 3, pp. 970-980, Sept. 2016.

[21] Z. Jin, L. Meng, R. Han *et al*., "Admittance-type RC-mode droop control to introduce virtual inertia in DC microgrids," in *Proceedings of 2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Cincinnati, USA, Oct. 2017, pp. 4107-4112.

[22] L. Herrera, W. Zhang, and J. Wang, "Stability analysis and controller design of DC microgrids with constant power loads," *IEEE Transactions Smart Grid*, vol. 8, no. 2, pp. 881-888, Mar. 2017.

[23] M. Cupelli, L. Zhu, and A. Monti, "Why ideal constant power loads are not the worst case condition from a control standpoint," *IEEE Transactions on Smart Grid*, vol. 6, no. 6, pp. 2596-2606, Oct. 2014.

[24] M. Cespedes, L. Xing, and J. Sun, "Constant-power load system stabilization by passive damping," *IEEE Transactions on Power Electronics*, vol. 26, no. 7, pp. 1832-1836, Jul. 2011.

[25] M. A. Bianchi, I. G. Zurbriggen, F. Paz *et al*., "Improving DC microgrids dynamic performance using a fast state-plane-based source-end controller," *IEEE Transactions on Power Electronics*, vol. 34, no. 8, pp. 8062-8078, Aug. 2019.

[26] Q. Xu, C. Zhang, C. Wen *et al*., "A novel composite nonlinear controller for stabilization of constant power load in DC microgrid," *IEEE Transactions on Smart Grid*, vol. 10, no. 1, pp. 752-761, Jan. 2019.

[27] X. Chang, Y. Li, X. Li *et al*., "An active damping method based on a supercapacitor energy storage system to overcome the destabilizing effect of instantaneous constant power loads in DC microgrids," *IEEE Transactions on Energy Conversion*, vol. 32, no. 1, pp. 36-47, Sept. 2016.

[28] M. Wu and D. D. Lu, "A novel stabilization method of LC input filter with constant power loads without load performance compromise in DC microgrids," *IEEE Transactions Industrial Electronics*, vol. 62, no. 7, pp. 4552-4562, Jul. 2015.

[29] M. N. Hussain, R. Mishra, and V. Agarwal, "A frequency-dependent virtual impedance for voltage regulating converters feeding constant power loads in a DC microgrids," *IEEE Transactions on Industry Applications*, vol. 54, no. 6, pp. 5630-5639, Nov. 2018.

[30] X. Lu, K. Sun, J. M. Guerrero *et al*., "Stability enhancement based on virtual impedance for DC microgrids with constant power loads," *IEEE Transactions on Smart Grid*, vol. 6, no. 6, pp. 2770-2783, Aug. 2015.

[31] S. Liu, P. Su, and L. Zhang, "A virtual negative inductor stabilizing strategy for DC microgrid with constant power loads," *IEEE Access*, vol. 6, pp. 59728-59741, Oct. 2018.

[32] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*. Berlin: Springer, 2001.

[33] Q. Xu, X. Hu, P. Wang *et al*., "A decentralized dynamic power sharing strategy for hybrid energy storage system in autonomous DC microgrid," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 7, pp. 5930-5941, Jul. 2017.

Mehran Jami received the B.Sc. degree from the University of Tehran, Tehran, Iran, and the M. Sc. degree from Tarbiat Modares University (TMU), Tehran, Iran, both in electrical engineering, in 2012 and 2014, respectively. He is now working toward a Ph.D. degree in the control of power systems at the University of Kurdistan, Sanandaj, Iran. He is currently a Member of the Smart/Micro Grids Research Center (SMGRC) at the University of Kurdistan. His research interests include modeling, analysis, design, and control of power electronics devices.

Qobad Shafiee received the Ph.D. degree in electrical engineering from the Department of Energy Technology, Aalborg University, Aalborg, Denmark, in 2014. He is currently an Assistant Professor, Associate Director of International Relations, and the Program Co-leader of the Smart/Micro Grids Research Center (SMGRC) at the University of Kurdistan, Sanandaj, Iran. His current research interests include modeling, energy management, control of power-electronics-based systems and microgrids, and model predictive and optimal control of modern power systems.

Hassan Bevrani received the Ph. D. degree in electrical engineering from Osaka University, Osaka, Japan, in 2004. Currently, he is a Full Professor and the Program Leader of Smart/Micro Grids Research Center (SMGRC) at the University of Kurdistan, Sanandaj, Iran. From 2016 to 2019, he was the Vice-chancellor for Research and Technology at the University of Kurdistan. His current research interests include smart grid operation and control, power systems stability and optimization, microgrid dynamics and control, and intelligent and robust control applications in power electric industry.