Reliability Evaluation of Wind Power Converter Under Fault-tolerant Control Scheme with Quantification of Temperature and Humidity Effects

Xueying Yu, Bo Hu, Kaigui Xie, Changzheng Shao, Yunjie Bai, Wenyuan Li, and Jinfeng Ding

***Abstract*—Wind power converter (WPC) is a key part of a wind power unit which delivers electric energy to power grid. Because of a large number of semiconductors, WPC has a high failure rate. This paper proposes a method to accurately evaluate the reliability of WPC, which is crucial for the design and maintenance of wind turbines. Firstly, the index of effective temperature (ET) is presented to quantify the effects of temperature and humidity on the semiconductor operation. A novel method is proposed to evaluate the lifetime and calculate the aging failure rates of the semiconductors considering the fluctuations of ET. Secondly, the failure mode and effect analysis (FMEA) of WPC is investigated based on the topology and control scheme. The conventional two-state reliability model of the WPC is extended to the multi-state reliability model where the partial working state under the fault-tolerant control scheme is allowed. Finally, a reliability evaluation framework is established to calculate the parameters of the WPC reliability model considering the variable failure rates and repair activities of semiconductors. Case studies are designed to verfify the proposed method using a practical wind turbine.**

***Index Terms*—Effective temperature (ET), fault-tolerant control scheme, humidity, reliability evaluation, wind power converter (WPC).**

I. Introduction

THE installed wind power generation worldwide has now achieved 743 GW, which is becoming one of the main generation resources [1], [2]. The reliability of wind power has important impacts on power grids [3]. For example, the faults at the Hornsea offshore wind farm in the UK triggered a significant blackout that affected about one million customers in 2019 [4].

Located between the generator and power grid, the wind power converter (WPC) converts and delivers electric energy to power grid, and is therefore a crucial part of wind turbines. Consisting of a large number of semiconductors, WPC is prone to aging and is therefore a frequent source of failure due to long-term outdoor application [5]. It is thus essential to accurately evaluate the reliability of the WPC, not only for the design, planning, and maintenance of wind turbines, but also for the reliability prediction and control of the wind power integrated power systems.

A number of pioneering studies have been conducted on this issue. Generally, evaluating the reliability of WPC includes two aspects: modeling the reliability of constituent elements (i.e., semiconductors), and building the global reliability model of WPC by combining the elements' model and taking into account the topology and control scheme.

In the element reliability modeling, many studies have been conducted on evaluating the reliability of semiconductors considering the aging effects caused by operating conditions (electrical operating conditions and climatic conditions) [6]-[8]. These generally fall into two categories: experience-based approach [9] - [12] and physics-of-failure-based approach [13]-[18]. The experience-based approach is usually based on statistics of failed products [9], [10]. It indicates that climatic conditions, especially temperature and humidity, have a significant contribution to the failures of semiconductors. It is generally applied to write handbooks as a guide to calculate the failure rates of semiconductors, which provide a base failure rate for a specific semiconductor and correction factors under operating conditions [11], [12]. However, this approach is inaccurate as it is application-independent and provides little information to quantify the effects of root causes on the reliability of semiconductors.

On the other hand, the physics-of-failure-based approach focuses on the failure mechanisms of semiconductors which could evaluate the reliability of semiconductors more accurately considering the aging process and quantify the effects of root causes. The existing studies aim to bridge the relationship between impact factors and thermal cycling in

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which the thermal failure mechanism is regarded as the dominant failure cause in semiconductors [6]. The effect of wind speed on thermal cycling is analyzed in [13], [14]. The reactive power effect is included in the impact factors of thermal cycling in [15], [16]. A complete thermal cycling calculation method considering different time constants is proposed in [17]. The thermal cycling is transformed into lifetime information in evaluating the reliability of semiconductors in [18]. However, this method only takes the electrical operating condition and ambient temperature into account based on the thermal failure mechanism. The other important impact factor of climatic conditions, humidity, is neglected, which has a significant effect on the reliability of semiconductors. Therefore, a new reliability evaluation method quantifying the effect of humidity is required.

In the reliability modeling of entire WPC, the existing method can be divided into three steps. First, the operating states of WPC are modeled using its topology and the failure mode and effects analysis (FMEA). Second, transition rates between all possible operating states are evaluated according to the failure rate and repair rate of semiconductors. Third, the probability of each operating state is calculated using a Markov model or other methods. Unfortunately, the existing researches have all assumed a two-state reliability model of WPC, in which WPC can operate only either in a perfect function state or in a complete failure state [11], [13], [15], [17], [19]-[21].

Yet, it is worth noting that many attempts are made to increase the reliability of WPC. The increasing attractiveness and demand is the fault-tolerant control scheme in which the WPC intends to maintain its operation with acceptable performance after some specific internal faults, and thus allows a reduction of energy conversion efficiency instead of complete failure when some unforeseen semiconductors fail [22]-[25]. However, the effect of the fault-tolerant control scheme on the reliability evaluation of WPC has not been considered. In this paper, the fault-tolerant control scheme of WPC is modeled to represent the reality of WPC operation more accurately.

Another deficiency in the existing research for the reliability evaluation of WPC is that the variable failure rates of semiconductors due to aging effects and repair activities are not considered.

Based on the aforementioned discussions, this paper proposes a method to more accurately evaluate the reliability of WPC. It extends the prior art by adding the following contributions.

1) The effective temperature (ET) is presented to quantify the effects of temperature and humidity on semiconductor reliability. Considering the fluctuations of ET during different operating conditions, a novel method is developed to estimate the lifetime and calculate the aging failure rates of semiconductors.

2) The FMEA method for WPC under the fault-tolerant control scheme is investigated. A multi-state model of WPC, in which an operating state representing the partial output capacity of WPC is allowed, is established to replace the conventional two-state model which has been assumed with inaccuracy in the WPC reliability modeling for a long time.

3) The variable failure rates of semiconductors due to aging effects and repair activities are considered in the WPC reliability evaluation using a sequential Monte Carlo simulation (SMCS) algorithm.

II. Reliability Evaluation of Semiconductors with Quantification of Temperature and Humidity Effects

It has been revealed that thermal cycling caused by thermal stress variation is one of the most critical failure causes in semiconductors [6]. In the existing research, only the temperature fluctuations caused by temperature in the environment and power loading are considered for thermal stress variation. However, the effect of humidity on thermal stress, which is another dominant impact factor, has not been considered. Therefore, in this section, ET is presented to quantify the effects of temperature and humidity on the thermal stress of semiconductors in WPC. Then, the thermal cyclings caused by modified thermal stress variation are transformed into the corresponding lifetime information in evaluating the reliability of semiconductors.

A. Concept of ET

In biometeorology, many studies have been conducted to evaluate the effects of changing weather conditions on human health. The major objective of them is to explore the relationship between biometeorological parameters and human health. It has been reported that human health depends largely on thermal comfort and resulting thermal stress [26]. The uppermost biometeorological parameters involved in thermal stress include temperature, humidity, wind speed, and solar radiation [27]. Therefore, various biometeorological indices have been proposed to quantify the effects of possibly biometeorological parameters on the thermal stress of human organisms. ET is one of the most widely used basic indices. It can measure the effects of temperature, humidity, and wind speed, and is applicable in both hot and cold situations [28]. It can be calculated by [29]:

$$ET_{T_a} = 85 - \frac{85 - T_a}{0.68 - 0.0014 \cdot RH + \dfrac{1}{1.76 + 1.4 V_w^{0.75}}} - 0.9 T_a (1 - 0.01 \cdot RH) \quad (1)$$

where ET_{T_a} is the ET in the environment; T_a is the temperature in the environment; RH is the relative humidity in the environment; and V_w is the wind speed.

To a certain extent, the reliability of semiconductors in WPC can be regarded as their health. Like human health, semiconductor reliability strongly depends on thermal stress and is sensitive to operating conditions due to long-term outdoor application. Moreover, the involved uppermost parameters for thermal stress of semiconductors under operating conditions are also temperature, humidity, and wind speed. Therefore, ET is introduced to quantify the effects of temperature and humidity on the thermal stress of semiconductors in WPC.

B. Calculating ET of Junction on Semiconductor Chips in WPC

The topology of WPC and cross-section view of a semi-

conductor in WPC are shown in Fig. 1, where IGBT stands for the insulated gate bipolar transistor. The temperature of the junction on the semiconductor chips is the highest operating temperature of semiconductors and its fluctuation directly affects the semiconductor lifetime. The calculation flowchart of ET of the junction on the semiconductor chips ET_{T_j} is shown in Fig. 2. The operating conditions including wind speed V_w, temperature T_a, and humidity RH in the ambient environment are used to calculate ET_{T_a} by (1). Then, the wind speed V_w is used to obtain generator output power P_{out}. Based on the power loss model, the power losses of semiconductors P_{loss} can be calculated. Finally, by inputting the ET_{T_a} into the thermal model, ET_{T_j} can be acquired.

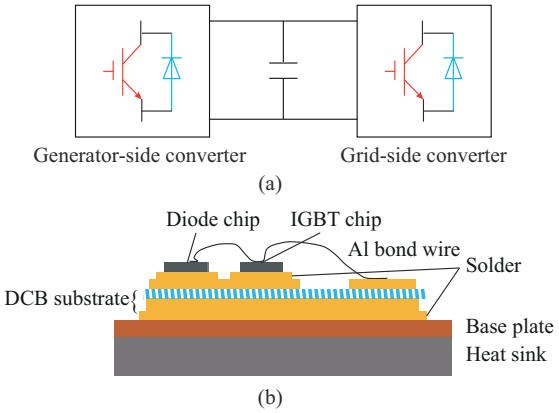

Fig. 1. Topology of WPC and cross-section view of a semiconductor in WPC. (a) Topology of WPC. (b) Cross-section view of a semiconductor.

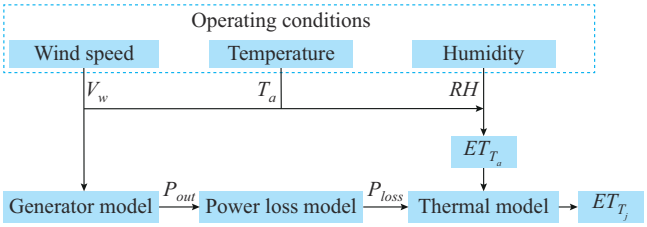

Fig. 2. Calculation flowchart of ET of junction on semiconductor chips ET_{T_j}.

1) Wind Power Output

The electric power produced by the wind turbine can be calculated based on the wind speed-power curve [30].

$$P_{out}=\begin{cases}0 & 0\le V_w\le V_{ci}\\ \left(A+BV_w+CV_w^2\right)P_r & V_{ci}<V_w\le V_r\\ P_r & V_r<V_w\le V_{co}\\ 0 & V_{co}<V_w\end{cases} \tag{2}$$

where V_{ci} is the cut-in speed; V_{co} is the cut-out speed; V_r is the rated speed; P_r is the rated power of the wind turbine; and A, B, and C are three constants defined in [30].

2) Power Losses of Semiconductors in WPC

According to the operating features of generators, the power losses of IGBTs and diodes can be divided into conduction losses and switching energy losses [11].

$$P_{loss}=P_{loss}^G+P_{loss}^D=P_{cd}^G+P_{sw}^G+P_{cd}^D+P_{sw}^D \tag{3}$$

where P_{cd} is the conduction losses; P_{sw} is the switching energy losses; and the superscripts G and D represent IGBT and diode, respectively.

The conduction losses and switching energy losses can be calculated by:

$$P_{cd}^G=U_{CE0}I_{om}\left(\frac{1}{2\pi}\pm\frac{M}{8}\cos\varphi\right)+r_{CE}I_{om}^2\left(\frac{1}{8}\pm\frac{M}{3\pi}\cos\varphi\right) \tag{4}$$

$$P_{sw}^G=\frac{1}{\pi}f_{sw}\left(E_{on}+E_{off}\right)\frac{V_{dc}I_{om}}{V_{ref}^GI_{ref}^G} \tag{5}$$

$$P_{cd}^D=U_{f0}I_{om}\left(\frac{1}{2\pi}\mp\frac{M}{8}\cos\varphi\right)+r_DI_{om}^2\left(\frac{1}{8}\mp\frac{M}{3\pi}\cos\varphi\right) \tag{6}$$

$$P_{sw}^D=\frac{1}{\pi}f_{sw}E_{rec}\frac{V_{dc}I_{om}}{V_{ref}^DI_{ref}^D} \tag{7}$$

where U_{CE0} and U_{f0} are the voltage drops on the IGBT and diode, respectively; r_{CE} and r_D are the resistances of IGBT and diode, respectively; M is the modulation coefficient; $\cos\varphi$ is the power factor; I_{om} is the peak of phase current; E_{rec} is the rated switching energy losses of the diode; E_{on} and E_{off} are the energy losses in the "ON" and "OFF" state, respectively; V_{ref} and I_{ref} are the reference commutation voltage and current, respectively; V_{dc} is the voltage of the semiconductor at the DC-side; and f_{sw} is the switching frequency.

Note that (4) and (6) contain signs of $\pm$ and $\mp$ where the upper sign should be used for grid-side converter calculations and the bottom one for generator-side converter calculations.

The peak of phase current I_{om} can be calculated by:

$$I_{om}=\frac{\sqrt{2}\,P_{out}}{\sqrt{3}\,U_l} \tag{8}$$

where U_l is the line voltage.

3) Calculating ET of Junction on Semiconductor Chips in WPC

The thermal model for calculating ET_{T_j} of the IGBT and diode is based on the thermal equivalent network. The thermal equivalent network of semiconductors in WPC is shown in Fig. 3, where ET_{T_h} is the ET of the heat sink; R_{thha} is thermal resistance from ambient to heat sink; R_{thch} is thermal resistance from the heat sink to case; and R_{thjc} is thermal resistance from case to junction. In Fig. 3, ET_{T_j} of the IGBT $ET_{T_j}^G$, ET_{T_j} of the diode chips $ET_{T_j}^D$, and ET of IGBT-based plate ET_{T_c} are shown, respectively, because they are closely related to the major failure mechanisms of the semiconductor.

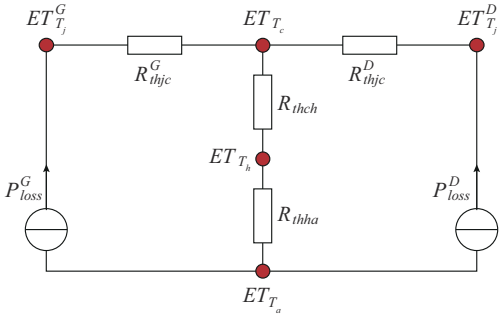

Fig. 3. Thermal equivalent network.

The $ET_{T_j}^G$ and $ET_{T_j}^D$ can be calculated by:

$$\begin{cases} ET_{T_h} = P_{loss} R_{thha} + ET_{T_a} \\ ET_{T_c} = P_{loss} R_{thch} + ET_{T_h} \\ ET_{T_j}^G = P_{loss}^G R_{thjc}^G + ET_{T_c} \\ ET_{T_j}^D = P_{loss}^D R_{thjc}^D + ET_{T_c} \end{cases} \tag{9}$$

C. Lifetime Estimation of Semiconductors Under Operating Conditions

The lifetime estimation of semiconductors is a general approach to evaluating the reliability of semiconductors considering aging effects. Estimating lifetime is based on counting thermal cyclings under operating conditions [17].

First, the thermal cyclings are counted under operating conditions. The rain flow counting method is applied to convert the randomly thermal stress variation to the regulated thermal cyclings which are transformed into the corresponding lifetime information. The counting results obtained from the rain flow counting method show that there are n classes counted ET_{T_j} cyclings of a semiconductor under operating conditions. The number of cyclings in the n^{th} class is N_n^a, and N_n^f is the corresponding number of cyclings to fully consume the lifetime. In the n^{th} class cycling, its corresponding information includes amplitude $dET_{T_{jm},n}$ and mean value $ET_{T_{jm},n}$, which are critical to the lifetime of semiconductors.

Then, the lifetime of semiconductors is estimated based on the aging test that follows Miner's rule [18]. In the lifetime estimation model, the cumulative damage AD is used to reflect aging effects on the lifetime of semiconductors.

$$AD = \sum_n \left(\frac{N_n^a}{N_n^f} \right)^{A_n^0} \tag{10}$$

where A_n^0 is the parameter in the n^{th} class.

A_n^0 and N_n^f can be calculated by:

$$A_n^0 = \alpha_1 \cdot dET_{T_j,n} + \alpha_2 \cdot ET_{T_{jm},n} + A_1 \tag{11}$$

$$N_n^f = A_2 \left(dET_{T_j,n} \right)^{\alpha_0} \tag{12}$$

where the parameters α_0, α_1, α_2, A_1, and A_2 are tested in the aging test [18].

The lifetime estimation of semiconductors L_s can be calculated by:

$$L_s = \frac{1}{AD} \tag{13}$$

D. Aging Failure Rate Calculation of Semiconductors Under Operating Conditions

In practice, the lifetime models and reliability of semiconductors have uncertainties with a certain range of variations. Therefore, the failure rate distribution of semiconductors should be obtained based on the lifetime of semiconductors with aging effects.

Generally, the Weibull distribution is always used to describe the failure distribution of semiconductors with aging effects, in which the shape parameter β and the scale parameter α are used to reflect aging effects. The aging failure rate of semiconductors at time t can be calculated by:

$$\lambda(t) = \alpha t^{\beta - 1} \tag{14}$$

The failure distribution $F(t)$ is the cumulative distribution function of the failure rate.

$$F(t) = \int_0^t \lambda(t)\,\mathrm{d}t = 1 - \mathrm{e}^{-\left(\frac{t}{\alpha}\right)^{\beta}} \tag{15}$$

The reliability function, which defines the probability of no failure before time t, can be expressed as:

$$R(t) = 1 - F(t) = \mathrm{e}^{-\left(\frac{t}{\alpha}\right)^{\beta}} \tag{16}$$

The reliability of semiconductors can also be characterized by mean time to failure (MTTF), which is the mathematical expectation of semiconductor lifetime.

$$MTTF = \int_0^{\infty} R(t)\,\mathrm{d}t \tag{17}$$

However, the MTTF will change with the operating conditions. The MTTF considering operating conditions can be represented as:

$$MTTF(t) = \int_{t_0}^{\infty} R(t|t_0)\,\mathrm{d}t = \mathrm{e}^{\left(\frac{t}{\alpha(t)}\right)^{\beta(t)}} \int_0^{\infty} \mathrm{e}^{-\left(\frac{L_s(t)+t_0}{\alpha(t)}\right)^{\beta(t)}}\,\mathrm{d}t \tag{18}$$

where t_0 is the period when the semiconductor has operated; $\beta(t)$ and $\alpha(t)$ are the time-dependent shape and scale parameters, respectively; and $L_s(t)$ is the lifetime estimation result at time t.

The time-dependent shape parameter $\beta(t)$ can be calculated by [31]:

$$\beta(t) = \frac{L_0}{t_0 + L_s(t)} \tag{19}$$

where L_0 is the lifetime provided by the manufacturer.

Then, the time-dependent scale parameter $\alpha(t)$ can be obtained by making:

$$MTTF(t) = L_s(t) \tag{20}$$

The aging failure rate of semiconductors at time t can be calculated by modified Weibull distribution with the time-dependent parameters by:

$$\lambda^{se,aging}(t) = \alpha(t) t^{\beta(t)-1} \tag{21}$$

III. Reliability Evaluation of WPC Under Fault-tolerant Control Scheme

Fault-tolerant control is a set of techniques that are developed to increase the equipment availability and reduce the risk of safety hazards in recent decades [32]. Like other high-reliability equipment, fault-tolerant control is being popularized in WPC as a cost-effective way to improve reliability. It enables the WPC to be in multiple partial working states more than the traditional two states (perfect function and complete failure states) in some failure modes. According to the operating features of the fault-tolerant converter, the multi-state model for reliability evaluation of WPC is developed. The SMCS algorithm is used to evaluate the reliability of WPC in this section.

A. FMEA of WPC Under Fault-tolerant Control Scheme

The fault-tolerant control scheme allows the WPC to have partial working states by preventing unplanned total stoppages. The control effects for generator-side and grid-side converters are different under various fault-tolerant control schemes. This sub-section only discusses the effect of a specific fault-tolerant control scheme on the operating states of WPC.

As shown in Fig. 4, the fault-tolerant converter consists of two six-switch three-phase converters in a back-to-back topology, in which each side comprises six IGBTs with the respective antiparallel diodes, and one additional triode AC switch (TRIAC), which remains open under normal operating conditions [22]. The proposed fault-tolerant control scheme in [22] allows WPC in the partial working state when a single-phase fault happens. In particular, when the IGBT in the same phase at the generator side fails, an alternative path for the current is available through the diodes. On the other hand, when the failure takes place at the grid-side, the included TRIAC reconfigures the circuit topology to increase an additional path for the current flowing in both directions. Consequently, the control scheme for the converter will change, and the energy conversion efficiency will reduce to ensure the safe operating of the converter when the WPC is in specific failure modes.

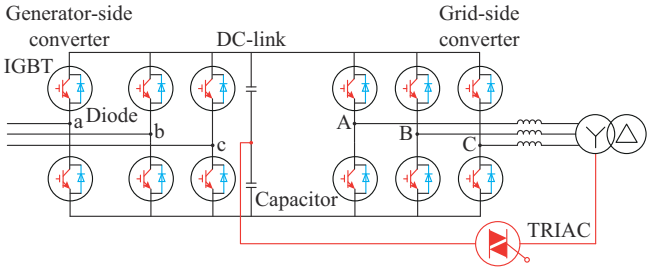

Fig. 4. Topology of a fault-tolerant converter.

The failure modes of WPC can be classified into four types according to the locations of failed semiconductors based on the fault-tolerant control scheme.

1) Mode 1: the failed semiconductors are in different phases.

2) Mode 2: the failed semiconductors are in the same phase in the generator-side converter.

3) Mode 3: the failed semiconductors are in the same phase in the grid-side converter.

4) Mode 4: there are no failed semiconductors.

Then, the operating states of WPC can be classified into different types: complete failure (State 1), partial working (State 2 and State 3), and perfect function (State 4). The details of classification are shown in Table I. State 2 and State 3 have different energy conversion efficiencies because of the control schemes for failure modes.

B. Multi-state Reliability Model of WPC Under Fault-tolerant Control Scheme

The FMEA for WPC is investigated under the fault-tolerant control scheme. The multi-state reliability model of WPC under fault-tolerant control scheme can be developed, as shown in Fig. 5.

TABLE I
CLASSIFICATION OF OPERATING STATES OF WPC UNDER FAULT-TOLERANT CONTROL SCHEME

Operating state	Operating state of WPC	Failure mode
Complete failure	State 1	Mode 1
Partial working	State 2	Mode 2
	State 3	Mode 3
Perfect function	State 4	Mode 4

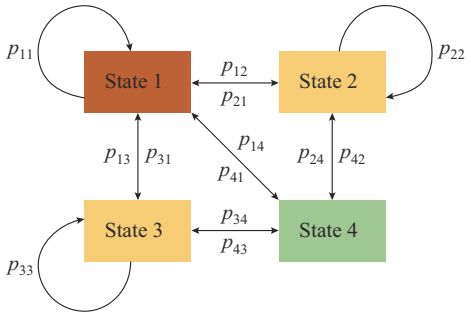

Fig. 5. Multi-state reliability model of WPC under fault-tolerant control scheme.

The curved arrow represents a transition from a state to itself (i.e., self-transition). The straight arrow represents a transition from a state to another state (i. e., mutual-transition). The transition rates p_{ij} (the probability of transitions from State i to State j over a specific residence time) between any states are presented by arrows in Fig. 5. For example, if only one semiconductor in phase a fails, the operating state of WPC will transfer from State 4 to State 2. Moreover, the transition rate p_{42} represents the transition rate from State 4 to State 2, which is the number of transitions from State 4 to State 2 in one year. The other parameters are defined in the same way.

Due to variable failure rates of semiconductors caused by aging effects and repair activities, it is difficult to obtain analytical solutions for the reliability evaluation of WPC. The SMCS algorithm is used to evaluate the reliability of WPC. The details will be expressed in the next subsection.

C. Reliability Evaluation of WPC Using SMCS Algorithm

The SMCS algorithm, for any type of probability distribution of semiconductor states, is applied to simulate the operating process of WPC. The flowchart for the reliability evaluation of WPC is shown in Fig. 6.

It is assumed that the k^{th} transition of the WPC operating state has taken place at time t_k and the time to the next operating state is x_k^{WPC}. The simulation proceeds in the following steps.

Step 1: set initial states of semiconductors.

Step 2: analyze the state of the q^{th} semiconductor S_q^{se}.

Step 3: obtain the duration of the q^{th} semiconductor state x_q^{se}.

For the aging semiconductor, the distribution of the failure rate is modified Weibull distribution $\lambda^{se,aging}$ in Section II.

$$x_q^{se}=\alpha\left(t_k\right)t_k-\ln\left(1-U\right)^{\frac{1}{\beta\left(t_k\right)}}-t_k \tag{22}$$

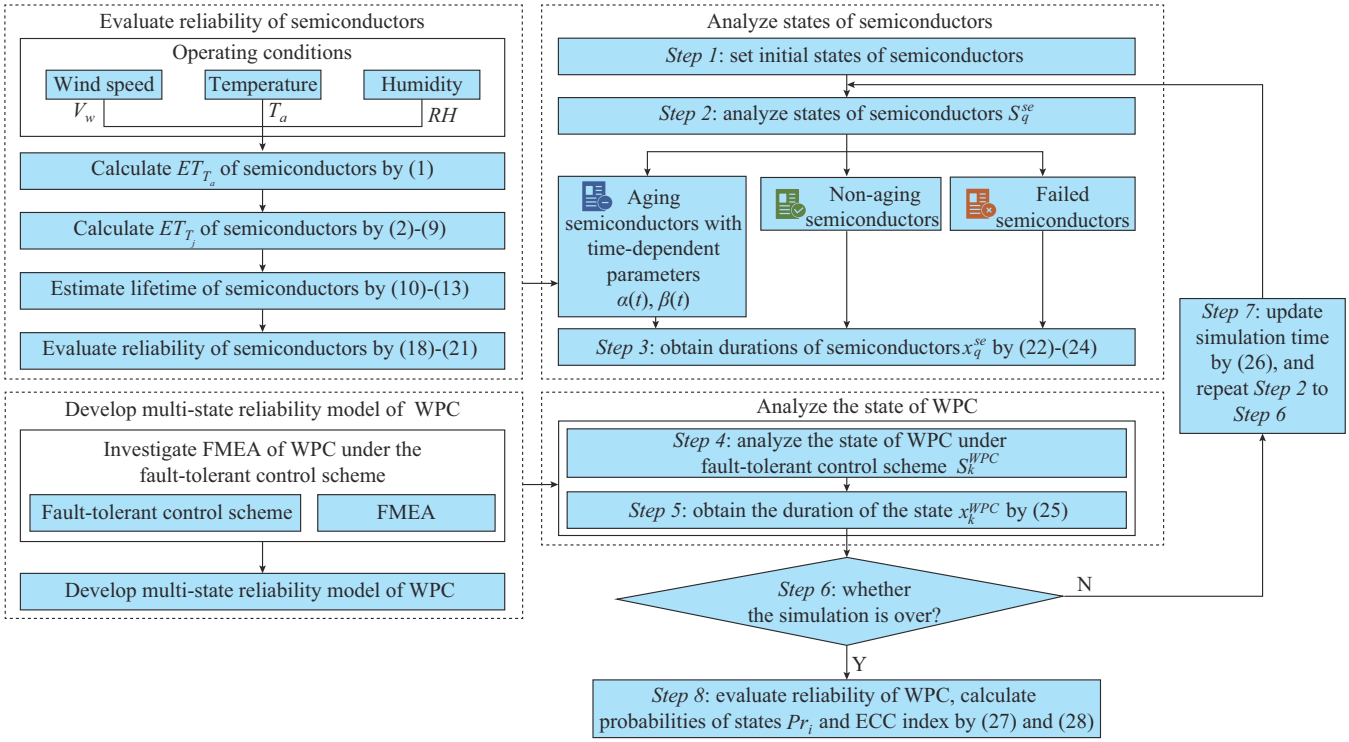

Fig. 6. Flowchart for reliability evaluation of WPC.

where U is a random number from a uniform distribution (0, 1].

The semiconductor is an unrepairable component. When the aged semiconductor fails, it will be directly replaced by a new semiconductor. Therefore, it should be noted that the semiconductor is thought to be aging from the initial state after it is repaired during the evaluation period.

For the non-aging semiconductor, the distribution of the failure rate is exponential.

$$x_q^{se} = -\frac{\ln U}{\lambda_q^{non,aging}} \tag{23}$$

where $\lambda_q^{non,aging}$ is the non-aging failure rate of the q^{th} semiconductor.

For the failed semiconductor, the repair time has exponential distribution.

$$x_q^{se} = -\frac{\ln U}{\mu_q} \tag{24}$$

where μ_q is the repair rate of the q^{th} semiconductor.

Step 4: analyze the current operating state of WPC S_k^{WPC} based on the states of semiconductors and FMEA under the fault-tolerant control scheme.

Step 5: obtain the duration of S_k^{WPC}, which can be determined by:

$$x_k^{WPC} = \min x_q^{se} \tag{25}$$

Step 6: judge whether the simulation is over. The coefficient of variation of the WPC reduced capacity due to semiconductor failures is used as the stopping rule. If the simulation is not over, go to *Step 7*. If the simulation is over, go to *Step 8*.

Then, repeat *Step 2* to *Step 6*.

Step 7: update simulation time.

$$t_{k+1} = t_k + x_k^{WPC} \tag{26}$$

Step 8: evaluate the reliability of WPC.

Record the duration of State i (SD_i), and then set $SD_i = SD_i + x_{k,i}^{WPC}$, where $x_{k,i}^{WPC}$ represents the duration of State i in the k^{th} transition.

The probability of State i can be calculated by:

$$Pr_i = \frac{SD_i}{t_k} \tag{27}$$

The expected conversion capacity (ECC) index is used to evaluate the reliability of WPC, which can be calculated by:

$$ECC = \sum_i C_i \cdot Pr_i \tag{28}$$

where C_i is the conversion capacity of WPC in State i.

In addition, the fault-tolerant control focuses on the semiconductor faults. There are also some requirements that should be considered such as the low-voltage ride-through (LVRT). To take the LVRT requirement for wind turbines with consideration of the reliability evaluation process, the calculation model for junction temperature of semiconductors is required to be expanded. Once this step is completed, the proposed reliability evaluation method can still be applied to evaluate the reliability of semiconductors and WPC with consideration of the LVRT. Satisfying wind turbine integration requirements like IEEE 1547 standard [33] is the same as the consideration of LVRT.

IV. Case Study

The proposed method is implemented on a 1.5 MW wind turbine with the prevailing topology, as shown in Fig. 4. The

details of the parameters of wind turbines and main semiconductors in WPC can be found in [11]. The cut-in, cut-out, and rated speeds of wind turbine are 3 m/s, 15 m/s, and 8 m/s, respectively. The operating conditions including wind speed, temperature, and RH in the environment at wind farms A and B in China in 2018 are shown in Fig. 7.

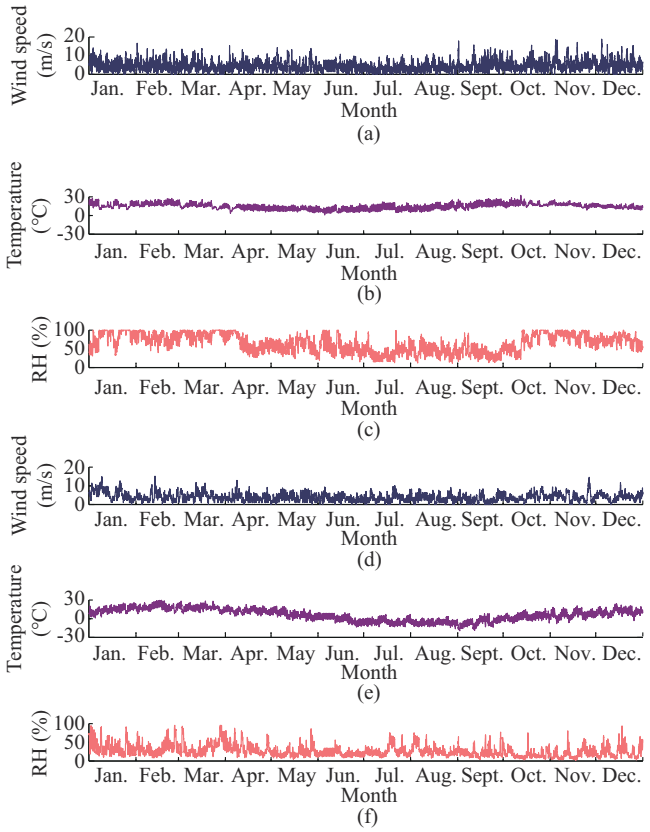

Fig. 7. Operating conditions at wind farms A and B in China in 2018. (a) Wind speed series at wind farm A. (b) Temperature series at wind farm A. (c) RH series at wind farm A. (d) Wind speed series at wind farm B. (e) Temperature series at wind farm B. (f) RH series at wind farm B.

The traditional method evaluates the reliability of WPC only by considering the effect of temperature on the reliability of semiconductors (thermal aging failure (TAF) based method) [18]. The proposed method in this paper considers the effects of temperature and humidity on the reliability of semiconductors and repair activities of semiconductors in the reliability evaluation of WPC. The reliability of the WPC is evaluated using the TAF method and the proposed method, respectively. The data statistics of operating conditions of wind farms A and B are given in Table II. It should be noted that the wind turbine used in the case studies is not the actual wind turbine at two farms.

TABLE II
DATA STATISTICS OF OPERATING CONDITIONS AT WIND FARMS A AND B

Wind farm	Wind speed (m/s)		Temperature (°C)		RH (%)	
	Mean	Standard deviation	Mean	Standard deviation	Mean	Standard deviation
A	4.75	0.99	14.56	3.61	65.61	6.16
B	3.91	0.28	6.18	0.48	27.07	11.61

A. Lifetime Estimation of Semiconductors Considering Effects of Temperature and Humidity

To analyze the effects of temperature and humidity on the semiconductor lifetime, the lifetime estimation results of semiconductors in WPC using the proposed method and TAF method at two wind farms are shown in Table III. It can be seen that lifetime estimation results are quite different when the effect of humidity is taken into account. Fortunately, the lifetime estimation results are close to the statistical results based on the common perception [9], [28]. Comparing the lifetime estimation results in Fig. 8, the effect of humidity on the lifetime of semiconductors at wind farm A is negative (when the humidity effect is taken into account, the lifetime estimation results are shorter). On the contrary, the effect of humidity on the lifetime of semiconductors at wind farm B is positive (when the humidity effect is taken into account, the lifetime estimation results are longer). The reason is that the wind speed and temperature at wind farm A are higher than those at wind farm B, which leads to the ET_{Tj} of semiconductors in WPC at wind farm A to be higher than that at wind farm B. It is consistent with the common perception, i.e., ET increases as humidity increases in high-temperature conditions. In the meanwhile, ET decreases as humidity increases in low-temperature conditions.

TABLE III
LIFETIME ESTIMATION RESULTS OF SEMICONDUCTORS IN WPC

Wind farm	Lifetime estimation result (year)							
	Proposed method (effects of temperature and humidity)				TAF method (effects of temperature effect)			
	Generator side		Grid side		Generator side		Grid side	
	IGBT	Diode	IGBT	Diode	IGBT	Diode	IGBT	Diode
A	1.47	14.73	3.23	3.80	1.96	19.85	4.27	5.05
B	12.21	136.76	28.59	34.10	6.60	67.70	15.01	17.82

To demonstrate the effects of temperature and humidity on the semiconductor lifetime, the different levels of temperature and humidity are executed to estimate the lifetime of the IGBT at the generator side, which is most prone to fail, based on the wind speed at two wind farms. It is apparent from Fig. 9 that the lifetime estimation results increase with humidity at the same temperature level. From Fig. 9(a), there are three scenarios that the lifetime estimation results are shorter than the results in Table III (operating condition). First, the temperature in the environment is 15 ℃, and the RH is more than 80%. Second, the temperature in the environment is 25 ℃, and the RH is more than 30%. Third, the temperature in the environment is 35 ℃, and the RH is more than 10%. The mean value of temperature and RH for the operating condition are 14.56 ℃ and 65.61%, respectively. On the other hand, from Fig. 9(b), the lifetime estimation results are shorter than the results in Table III (operating condition) when the temperature is higher than 5 ℃. The mean value of temperature and RH for the operating condition are 6.18 ℃ and 27.07%, respectively. Taken together, these results suggest that the temperature and humidity have non-negligible effects on the lifetime estimation results of semiconductors. However, whether the effect is positive or nega-

tive depends on the operating conditions.

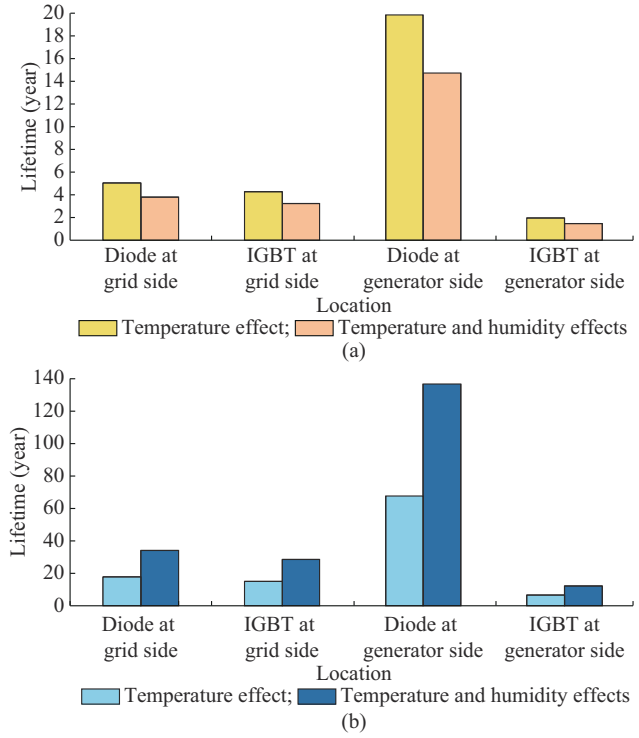

Fig. 8. Comparison of lifetime estimation results. (a) WPC at wind farm A. (b) WPC at wind farm B.

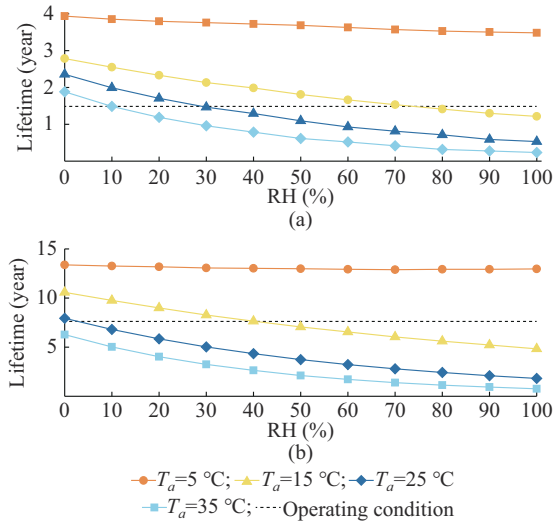

Fig. 9. Effects of different levels of temperature and humidity on semiconductor lifetime estimation results. (a) Wind farm A. (b) Wind farm B.

B. Reliability Evaluation of WPC Under Fault-tolerant Control Scheme

The fault-tolerant control scheme in [22] is used in this paper. The FMEA for WPC under fault-tolerant control scheme is investigated, as shown in Table IV. The conversion efficiency of the WPC is limited to 93.9% when the failure mode is Mode 2. The conversion efficiency of the WPC decreases to 76.2% when the failure mode is Mode 3. L_0 is 25 years and t_0 is 10 years. The non-aging failure rate and repair rate of semiconductors in WPC is 0.3 occurrence per year and 53 occurrence per year, respectively [34], [35]. The failure rate of capacitors in the DC link is 0.0004 occurrence per year [11]. The failure rate of the control system is 0.05 occurrence per year [10], respectively.

TABLE IV
FMEA FOR WPC UNDER FAULT-TOLERANT CONTROL SCHEME

Operation state	Operation state of WPC	Failure mode	Conversion efficiency (%)
Complete failure	State 1	Mode 1	0
Partial working	State 2	Mode 2	93.9
	State 3	Mode 3	76.2
Perfect function	State 4	Mode 3	100.0

To study the effects of humidity and temperature and repair activities of semiconductors on the reliability of WPC, the following four cases considering difference effects are shown in Table V.

TABLE V
FOUR CASES CONSIDERING DIFFERENT EFFECTS

Case	Humidity	Temperature	Repair activity	Fault-tolerant control scheme
1		√		
2		√		√
3		√	√	
4	√	√	√	

1) Case 1 (traditional method): only the effect of temperature on the reliability of semiconductors is considered. The WPC only has two states in which the fault-tolerant control scheme is not considered.

2) Case 2: only the effect of temperature on the reliability of semiconductors is considered.

3) Case 3: the effects of temperature on the reliability of semiconductors and repair activities of semiconductors are considered.

4) Case 4 (proposed method): the effects of temperature and humidity on the reliability of semiconductors and repair activities of semiconductors are considered.

The reliability evaluation results of WPC are shown in Table VI.

The probabilities of states for the cases are shown in Fig. 10. The results are close to the statistical results. It can be observed that the probability of the complete failure state decreases sharply under the fault-tolerant control scheme. For example, the probability of the complete failure state decreases from 0.0389 to 0.0036 in Case 4 at wind farm A. Therefore, the fault-tolerant control scheme has a great effect on improving the reliability of WPC.

The reliability indices of WPC and computational time using the traditional and proposed methods are compared, as shown in Table VII. The additional computational burden for improving the accuracy of reliability indices using the proposed methods is acceptable. In addition, the reliability evaluation results show that the difference in the probability of perfect function is 1.52% with consideration of humidity and

thermal impacts and consideration of thermal impact at wind farm A. The differences at wind farm B are 2.63%. It can be believed that humidity affects the multi-state probability of WPC more pronounced. The results of two wind farms show that the deviation of the same result at wind farm A is more than that at wind farm B. It provides important insights that humidity has a more significant effect under higher temperature.

TABLE VI
RELIABILITY EVALUATION RESULTS OF WPC

Condition	Probability in Case 1		Probability in Case 2		Probability in Case 3		Probability in Case 4	
	Wind farm A	Wind farm B	Wind farm A	Wind farm B	Wind farm A	Wind farm B	Wind farm A	Wind farm B
Complete failure, State 1	0.0130	0.0130	0.0006	0.0006	0.0010	0.0010	0.0030	0.0040
Partial working, State 2			0.0030	0.0030	0.0050	0.0050	0.0140	0.0160
Partial working, State 3			0.0040	0.0040	0.0060	0.0060	0.0170	0.0190
Perfect function, State 4	0.9810	0.9870	0.9930	0.9930	0.9880	0.9880	0.9660	0.9610
ECC	1.4715	1.4805	1.4976	1.4976	1.4960	1.4960	1.4863	1.4882

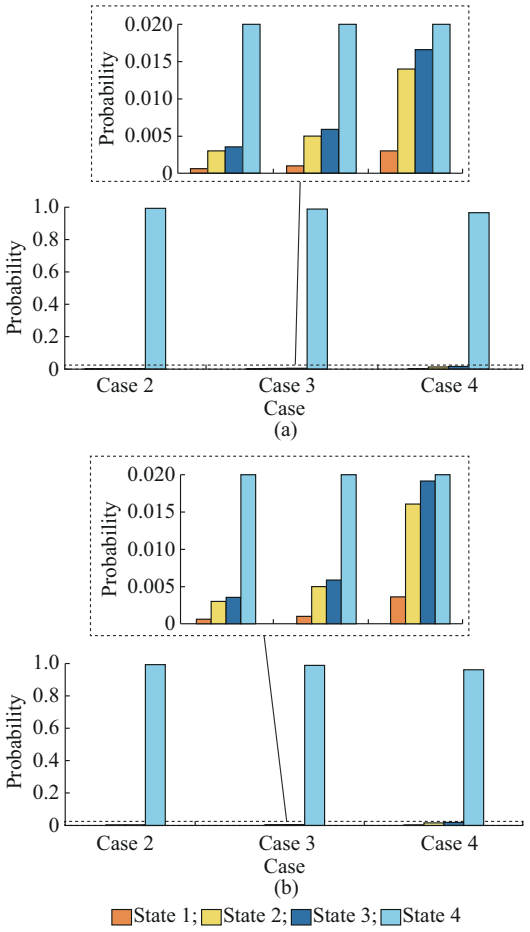

Fig. 10. Probabilities of states for cases. (a) WPC at wind farm A. (b) WPC at wind farm B.

The simulation results show that the effects of temperature and humidity, fault-tolerant control scheme, and repair activities are all important for evaluating WPC reliability. If the operating conditions and repair activities are not taken into account, the reliability evaluation of WPC might be overly optimistic. If the fault-tolerant control scheme is not taken into account, the reliability evaluation of WPC might be overly pessimistic. These can cause a serious effect on the planning and operation of the WPC with renewable energy integration.

V. CONCLUSION

A method for the reliability evaluation of WPC under the fault-tolerant control scheme with the quantification of temperature and humidity effects is developed. The ET index is presented to quantify the effects of temperature and humidity. The conventional two-state reliability model of WPC is extended to the multi-state reliability model under the fault-tolerant control scheme. By capturing the failure rate variations of semiconductors caused by aging effects and repair activities, the WPC reliability is evaluated using the proposed SMCS algorithm combined with the FMEA of WPC.

The following observations are made from the simulation results.

1) The effect of humidity on semiconductor reliability cannot be ignored. The correlation between humidity effect and lifetime should be analyzed considering the operating conditions.

2) The reliability evaluation for WPC is overly optimistic if the operating conditions and failure rate variations of semiconductors are not taken into account, which may result in a misleading judgment in decision-making.

TABLE VII
COMPARISON OF MULTI-STATE PROBABILITY

Method	Wind farm A						Wind farm B					
	Probability				ECC	Computational time (s)	Probability				ECC	Computational time (s)
	State 1	State 2	State 3	State 4			State 1	State 2	State 3	State 4		
Traditional method	0.013			0.981	1.4715	47.15	0.013			0.987	1.4805	46.03
Proposed method	0.003	0.014	0.017	0.966	1.4863	108.63	0.004	0.016	0.019	0.961	1.4882	109.98
Difference (%)	76.92			1.52	1	130.39	69.23			2.63	0.5	138.93

Although the major factors missed in previous works (such as the humidity effect, fault-tolerant control scheme, and failure rate variations of semiconductors) are addressed in this paper, there is still room for further investigation into the failure mechanism of WPC. This will be our task in future research.

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